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Application Note AN4146

Design Guidelines for Quasi-Resonant Converters Using FSCQ-series Fairchild Power Switch (FPS™)

Abstract

In general, a Quasi-Resonant Converter (QRC) shows lower EMI and higher power conversion efficiency compared to the conventional hard switched converter with a fixed switching frequency. Therefore, it is well suited for color TV applications that are noise sensitive. This application note presents practical design considerations of Quasi-Resonant Converters for color TV applications employing FSCQ-series FPS™ (Fairchild Power Switch). It includes designing the transformer, output filter and sync network, selecting the components and closing the feedback loop. The step-by-step design procedure described in this application note will help engineers design Quasi-Resonant Converter easily. To make the design process more efficient, a software design tool, **FPS design assistant** which contains all the equations described in this application note, is also provided. The design procedure is verified through an experimental prototype converter.

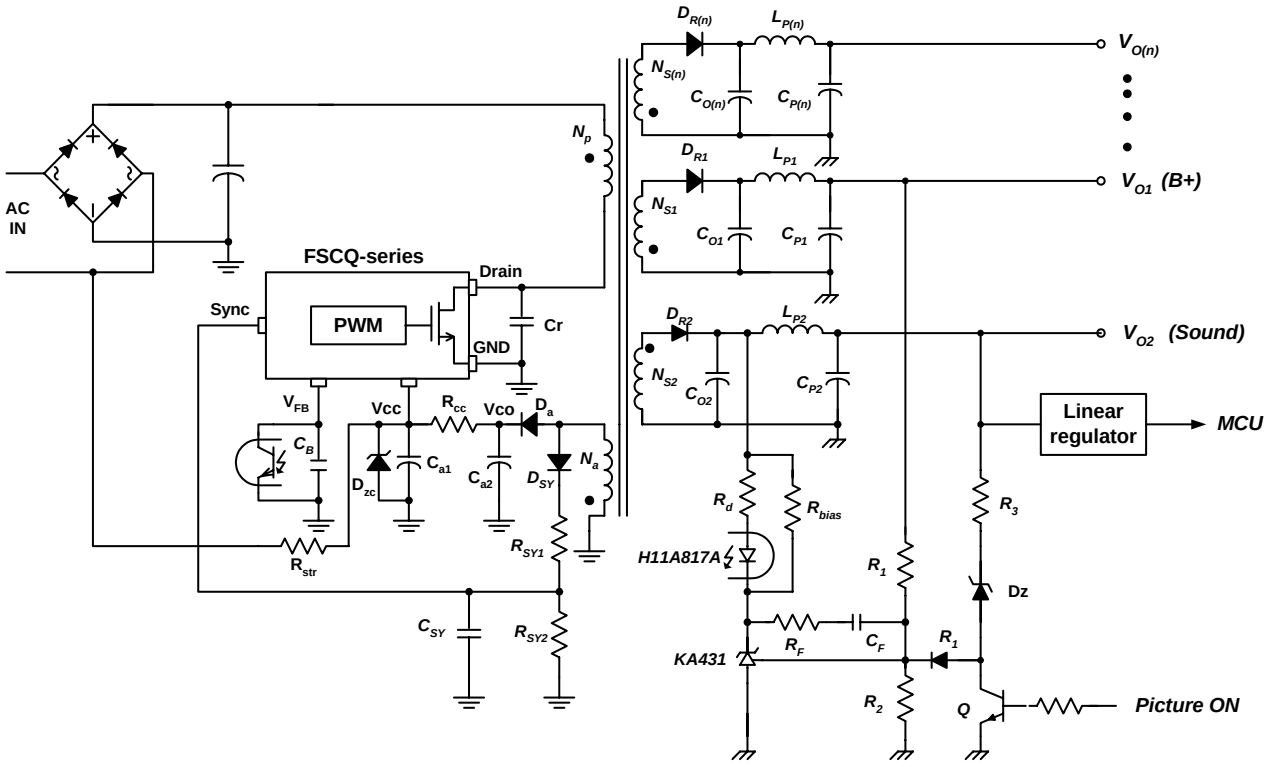


Figure 1. Basic Quasi-Resonant Converter (QRC) Using FPS (Color TV Application)

1. Introduction

The FSCQ-series FPS™ (Fairchild Power Switch) is an integrated Pulse Width Modulation (PWM) controller and Sense FET specifically designed for Quasi-resonant off-line Switch Mode Power Supplies (SMPS) with minimal external components. Compared with discrete MOSFET and PWM controller solution, it can reduce total cost, component count, size and weight, while simultaneously increasing efficiency, productivity, and system reliability.

Figure 1 shows the basic schematic of an FPS based Quasi-Resonant Converter for the color TV application, which also serves as the reference circuit for the design process described in this application note. An experimental converter from the design example has been built and tested to show the validity of the design procedure.

2. Step-by-step Design Procedure

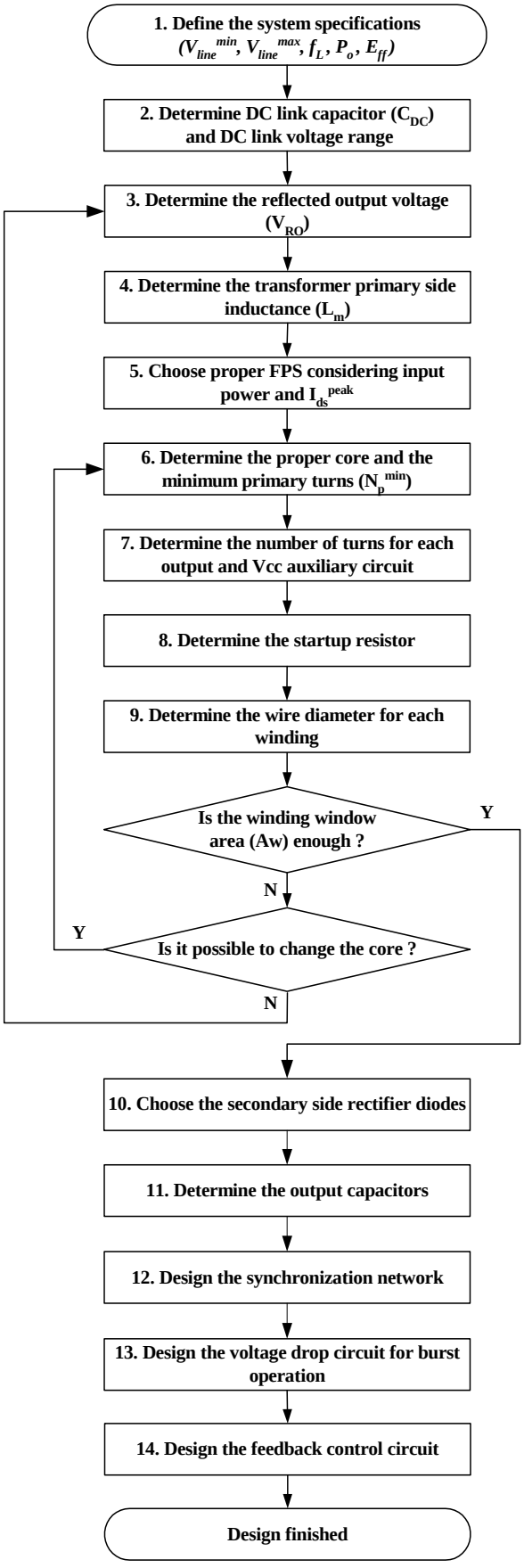


Figure 2. Flow Chart of Design Procedure

In this section, a design procedure is presented using the schematic of Figure 1 as a reference. Figure 2 illustrates the design flow chart. The detailed design procedures are as follows:

[STEP-1] Define the system specifications

- Line voltage range (V_{line}^{min} and V_{line}^{max}).
- Line frequency (f_L).
- Maximum output power (P_o).
- Estimated efficiency (E_{ff}) : The power conversion efficiency must be estimated to calculate the maximum input power. If no reference data is available, set E_{ff} = 0.7~0.75 for low voltage output applications and E_{ff} = 0.8~0.85 for high voltage output applications. In the case of Color TV applications, the typical efficiency is 80~83%.

With the estimated efficiency, the maximum input power is given by

$$P_{in} = \frac{P_o}{E_{ff}} \quad (1)$$

For multiple output SMPS, the load occupying factor for each output is defined as

$$K_{L(n)} = \frac{P_{o(n)}}{P_o} \quad (2)$$

where $P_{o(n)}$ is the maximum output power for the n-th output. For single output SMPS, $K_{L(1)}$=1. It is assumed that V_{o1} is the reference output that is regulated by the feedback control in normal operation.

[STEP-2] Determine DC link capacitor (C_{DC}) and the DC link voltage range.

Typically, the DC link capacitor is selected as 2-3uF per watt of input power for universal input range (85-265Vrms) and 1uF per watt of input power for European input range (195V-265Vrms). With the DC link capacitor selected, the minimum DC link voltage is obtained as

$$V_{DC}^{min} = \sqrt{2 \cdot (V_{line}^{min})^2 - \frac{P_{in} \cdot (1 - D_{ch})}{C_{DC} \cdot f_L}} \quad (3)$$

where C_{DC} is the DC link capacitor and D_{ch} is the duty cycle ratio for C_{DC} to be charged as defined in Figure 3, which is typically about 0.2. P_{in}, V_{line}^{min} and f_L are specified in STEP-1.

The maximum DC link voltage is given as

$$V_{DC}^{max} = \sqrt{2} V_{line}^{max} \quad (4)$$

where V_{line}^{max} is specified in STEP-1.

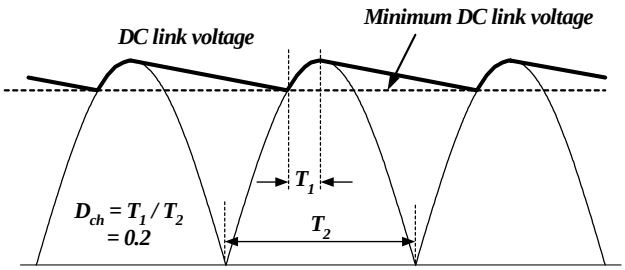


Figure 3. DC Link Voltage Waveform

[STEP-3] Determine the reflected output voltage (V_{RO})

Figure 4 shows the typical waveforms of the drain voltage of Quasi-resonant flyback converter. When the MOSFET is turned off, the DC link voltage (V_{DC}) together with the output voltage reflected to the primary (V_{RO}) is imposed on the MOSFET and the maximum nominal voltage across the MOSFET (V_{ds}^{nom}) is

$$V_{ds}^{nom} = V_{DC}^{max} + V_{RO} \quad (5)$$

where V_{DC}^{max} is as specified in equation (4). By increasing V_{RO}, the capacitive switching loss and conduction loss of the MOSFET are reduced. However, this increases the voltage stress on the MOSFET as shown in Figure 4. Therefore, V_{RO} should be determined by a trade-off between the voltage margin of the MOSFET and the efficiency. It is typical to set V_{RO} as 120~180V so that V_{ds}^{norm} is 490~550V (75~85% of MOSFET rated voltage).

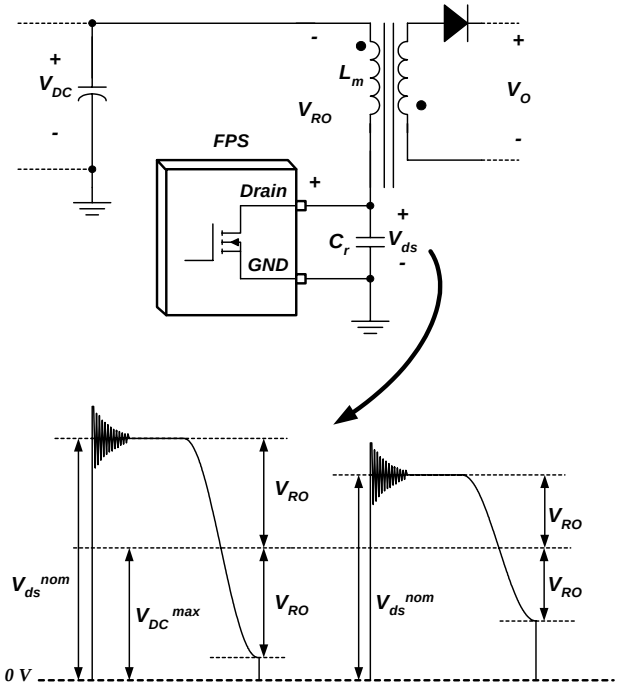


Figure 4. The Typical Waveform of MOSFET Drain Voltage for Quasi Resonant Converter

[STEP-4] Determine the transformer primary side inductance (L_m)

Figure 5 shows the typical waveforms of MOSFET drain current, secondary diode current and the MOSFET drain voltage of a Quasi-Resonant Converter. During T_{OFF}, the current flows through the secondary side rectifier diode and the MOSFET drain voltage is clamped at (V_{DC}+V_{RO}). When the secondary side current reduces to zero, the drain voltage begins to drop because of the resonance between the effective output capacitor of the MOSFET and the primary side inductance (L_m). To minimize the switching loss, the FSCQ-series is designed to turn on the MOSFET when the drain voltage reaches its minimum voltage (V_{DC} -V_{RO}).

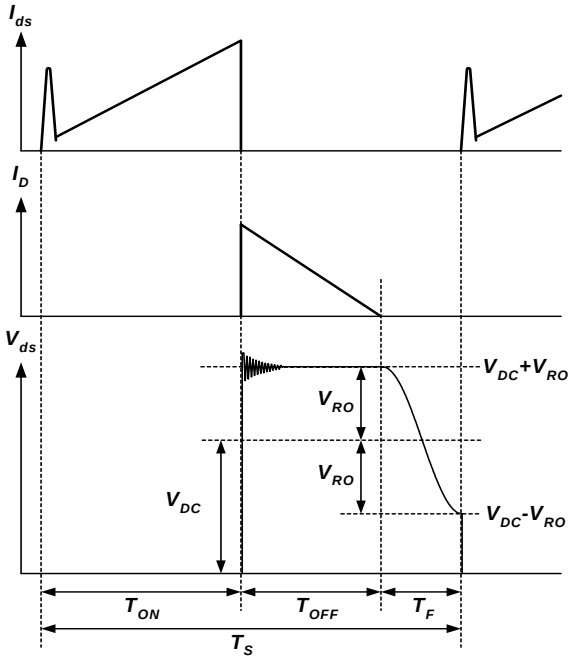


Figure 5. Typical Waveforms of Quasi-Resonant Converter

To determine the primary side inductance (L_m), the following variables should be determined beforehand.

- **The minimum switching frequency (f_s^{min}) :** The minimum switching frequency occurs at the minimum input voltage and full load condition, which should be higher than the minimum switching frequency of FPS (20kHz). By increasing f_s^{min}, the transformer size can be reduced. However, this results in increased switching losses. Therefore determine f_s^{min} by a trade-off between switching losses and transformer size. Typically, f_s^{min} is set to be around 25kHz.
- **The falling time of the MOSFET drain voltage (T_F) :** As shown in Figure 5, the MOSFET drain voltage fall time is half of the resonant period of the MOSFET's effective output capacitance and primary side inductance. By increasing T_F, EMI can be reduced. Meanwhile, this forces an increase of the resonant capacitor (*Cr*) resulting in increased switching losses. The typical value for T_F is 2-2.5us.

After determining f_s^{min} and T_F, the maximum duty cycle is calculated as

$$D_{max} = \frac{V_{RO}}{V_{RO} + V_{DC}^{min}} \cdot (1 - f_s^{min} \times T_F) \quad (6)$$

where V_{DC}^{min} is specified in equation (3) and V_{RO} is determined in STEP-3.

Then, the primary side inductance is obtained as

$$L_m = \frac{(V_{DC}^{min} \cdot D_{max})^2}{2 \cdot f_s^{min} \cdot P_{in}} \quad (7)$$

where P_{in}, V_{DC}^{min} and D_{max} are specified in equations (1), (3), and (6), respectively and f_s^{min} is the minimum switching frequency.

Once L_m is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as

$$I_{ds}^{peak} = \frac{V_{DC}^{min} D_{max}}{L_m f_s^{min}} \quad (8)$$

$$I_{ds}^{rms} = \sqrt{\frac{D_{max}}{3}} \cdot I_{ds}^{peak} \quad (9)$$

where V_{DC}^{min}, D_{max} and L_m are specified in equations (3), (6) and (7), respectively and f_s^{min} is the minimum switching frequency.

[STEP-5] Choose the proper FPS considering input power and peak drain current.

With the resulting maximum peak drain current of the MOSFET (I_{ds}^{peak}) from equation (8), choose the proper FPS whose the pulse-by-pulse current limit level (I_{LIM}) is higher than I_{ds}^{peak}. Since FPS has ± 12% tolerance of I_{LIM}, there should be some margin for I_{LIM} when choosing the proper FPS device. Table 1 shows the lineups of FSCQ-series with rated output power and pulse-by-pulse current limit.

Maximum Output Power					
PRODUCT	230VAC ±15%	85-265Vac	I_{LIM} (A)		
			Min	Typ	Max
FSCQ0565RT	70 W	60 W	3.08	3.5	3.92
FSCQ0765RT	100 W	85 W	4.4	5	5.6
FSCQ0965RT	130 W	110 W	5.28	6	7.84
FSCQ1265RT	170 W	140 W	6.16	7	7.84
FSCQ1465RT	190 W	160 W	7.04	8	8.96
FSCQ1565RT	210 W	170 W	7.04	8	8.96
FSCQ1565RP	250 W	210 W	10.12	11.5	12.88

Table 1. FPS Lineups with Rated Output Power

[STEP-6] Determine the proper core and the minimum primary turns.

Table 2 shows the commonly used cores for C-TV application for different output powers. When designing the transformer, consider the maximum flux density swing in normal operation (ΔB) as well as the maximum flux density in transient (B_{max}). The the maximum flux density swing in normal operation is related to the hysteresis loss in the core while the maximum flux density in transient is related to the core saturation.

With the chosen core, the minimum number of turns for the transformer primary side to avoid the over temperature in the core is given by

$$N_P^{min} = \frac{L_m I_{ds}^{peak}}{\Delta B A_e} \times 10^6 \quad (10)$$

where L_m is specified in equation (7), I_{ds}^{peak} is the peak drain current specified in equation (8), A_e is the cross-sectional area of the transformer core in mm^2 as shown in Figure 6 and ΔB is the maximum flux density swing in tesla. If there is no reference data, use ΔB =0.25~0.30 T.

Since the MOSFET drain current exceeds I_{ds}^{peak} and reaches I_{LIM} in a transient or fault condition, the transformer should be designed not to be saturated when the MOSFET drain current reaches I_{LIM} . Therefore, the maximum flux density (B_{max}) when drain current reaches I_{LIM} should be also considered as

$$N_P^{min} = \frac{L_m I_{LIM}}{B_{max} A_e} \times 10^6 \quad (11)$$

where L_m is specified in equation (7), I_{LIM} is the pulse-by-pulse current limit, A_e is the cross-sectional area of the core in mm^2 as shown in Figure 6 and B_{max} is the maximum flux density in tesla. Figure 7 shows the typical characteristics of ferrite core from TDK (PC40). Since the core is saturated at low flux density as the temperature goes high, consider the high temperature characteristics. If there is no reference data, use B_{max} =0.35~0.4 T.

The primary turns should be determined as less than N_p^{min} values obtained from equation (10) and (11).

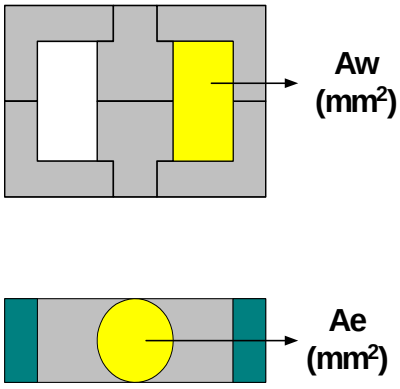


Figure 6. Window Area and Cross Sectional Area

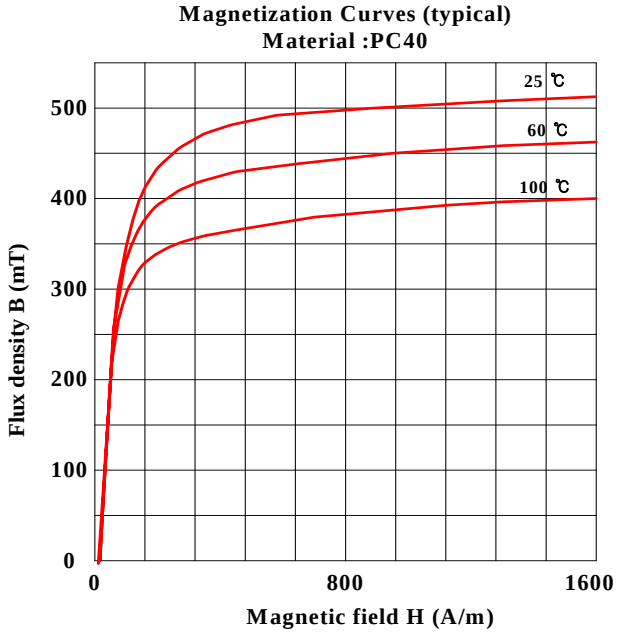


Figure 7. Typical B-H Characteristics of Ferrite Core (TDK/PC40)

Output Power	Core
70-100W	EER35
100-150W	EER40 EER42
150-200W	EER49

Table 2. Commonly Used Cores for C-TV Applications

[STEP-7] Determine the number of turns for each output and Vcc auxiliary circuit

Figure 8 shows the simplified diagram of the transformer. It is assumed that V_{o1} is the reference output that is regulated by the feedback control in normal operation. It is also assumed that linear regulator is connected to V_{o2} to supply a stable voltage for MCU.

First, calculate the turns ratio (n) between the primary winding and reference output (V_{o1}) winding as a reference as in

$$n = \frac{V_{R0}}{V_{o1} + V_{F1}} \qquad (12)$$

where V_{RO} is determined in STEP-3 and V_{o1} is the reference output voltage and V_{F1} is the forward voltage drop of diode (D_{R1}).

Then, determine the appropriate integer for N_{s1} so that the resulting N_p is larger than N_p^{min} as

$$N_p = n \cdot N_{s1} > N_p^{min} \qquad (13)$$

where n is obtained in equation (12) and N_p and N_{s1} are the number of turns for the primary side and the reference output, respectively.

The number of turns for the other output (n-th output) is determined as

$$N_{s(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \cdot N_{s1} \qquad (14)$$

where $V_{o(n)}$ is the output voltage and $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage drop of the n-th output, respectively.

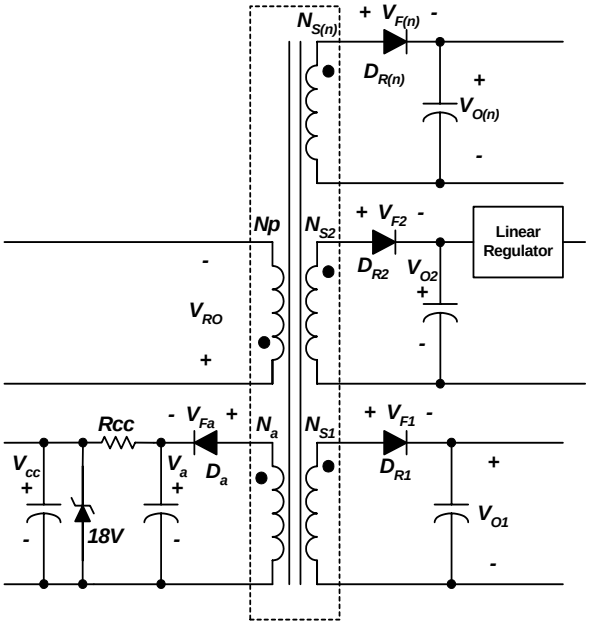


Figure 8. Simplified Diagram of the Transformer

- Vcc winding design : As shown in Figure 9, FSCQ-series drops all the outputs including the Vcc auxiliary voltage (V_a) in standby mode to minimize the power consumption. Because the Vcc auxiliary voltage (V_a) changes a over wide range, a regulation circuit using zener diode is typically used to provide a stable supply voltage (Vcc) for FPS in normal operation, as shown in Figure 8. It is typical to design the regulation circuit so that the Vcc voltage is regulated as 18V in normal operation and is above Vcc stop voltage (9V) by 2~3V in standby operation as shown in Figure 9. After FSCQ-series enters into standby mode, the current consumed by FPS drops below 500uA and the voltage drop across R_{cc} is negligible.

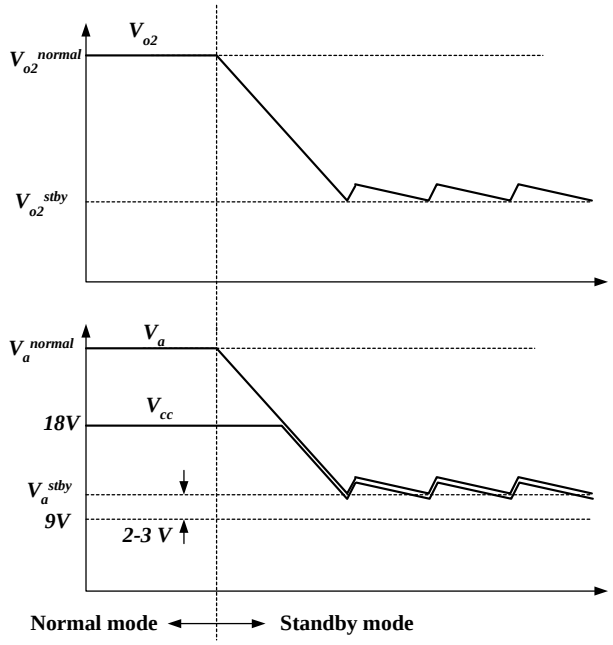


Figure 9. Output Voltage Drop in Standby Mode

In standby mode, V_{o2} is regulated by the feedback control and the voltage drop ratio of the V_{o2} winding is defined in

$$K_{drop} = \frac{V_{02}^{stby} + V_{F2}}{V_{02}^{normal} + V_{F2}} \quad (15)$$

where V_{F2} is the diode forward voltage drop of the D_{R2}, and $V_{o2}^{normal}$and V_{o2}^{stby} are the output voltages of V_{o2} in normal mode and standby mode, respectively, as shown in Figure 9.

Assuming that the Vcc auxiliary voltage (V_a) is reduced with the ratio of K_{drop}, V_a in normal mode is obtained as

$$V_a^{normal} = \frac{V_a^{stby} + V_{Fa}}{K_{drop}} - V_{F2} \quad (16)$$

where V_a^{stby} is the minimum voltage of V_a in standby mode, which should be larger than Vcc stop voltage of FPS (typically 9V). Notice that the operating current is reduced in standby mode and therefore the voltage drop across R_{cc} is negligible. It is typical to have a voltage margin of 2-3V when determining V_a^{stby}.

After determining V_a^{normal}, the number of turns for the Vcc auxiliary winding (N_a) is obtained as

$$N_a = \frac{V_a^{normal} + V_{Fa}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (17)$$

where V_{Fa} is the forward voltage drop of D_a as defined in Figure 8.

- Vcc drop resistor (R_{cc}) : The current consumed by FPS in normal operation is given by

$$I_{cc} = I_{op} + I_{drv} \quad (18)$$

where I_{op} and I_{drv} are the currents required for IC operation and MOSFET gate drive, respectively. I_{op} is given in the data sheet and I_{drv} is obtained as

$$I_{drv} = V_{cc} \cdot C_{iss} \cdot f_s \quad (19)$$

where C_{iss} is the input capacitance of the MOSFET and f_s is the switching frequency. When considering I_{drv}, it is typical to assume that V_{cc} is Vz (18V) and f_s is 90kHz.

The condition for the Vcc drop resistor (R_{cc}) is given by

$$R_{cc} < \frac{V_{co}^{normal} - V_z}{I_{cc}} \quad (20)$$

The heat dissipation of R_{cc} in normal operation is given by

$$P_a = \frac{(V_{co}^{normal} - V_z)^2}{R_{cc}} \quad (21)$$

where V_z is the zener breakdown voltage (typically 18V).

When a large voltage drop of more than 20V is required, application circuit shown in Figure 11 is preferred to minimize the power dissipation in the voltage drop circuit.

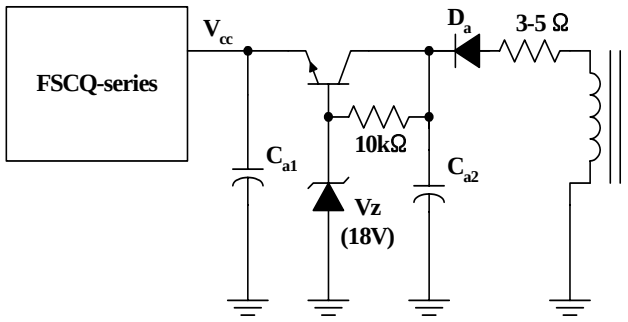


Figure. 10 Vcc Auxiliary Circuit for a Large Voltage Drop

[STEP-8] Determine the startup resistor

Figure 10 shows the typical circuit of Vcc winding for FSCQ-series. Initially, FPS consumes only startup current (max 50uA) before it begins switching. Therefore, the current supplied through the startup resistor (R_{str}) can charge the capacitors C_{a1} and C_{a2} while supplying startup current to FPS. When Vcc reaches start voltage of 15V (V_{START}), FPS begins switching and the current consumed by FPS increases. Then, the current required by FPS is supplied from the transformer's auxiliary winding.

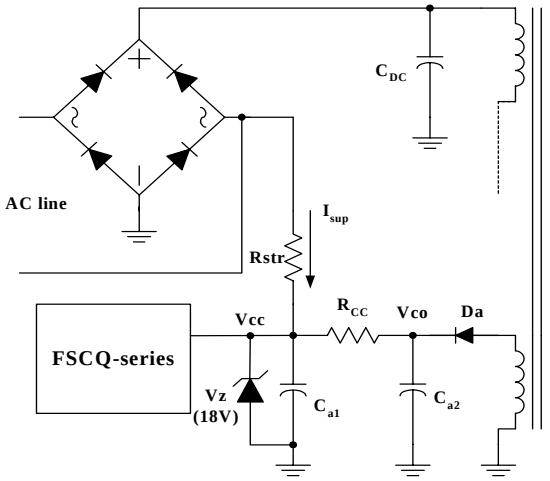


Figure. 11 Startup and Vcc Auxiliary Circuit

- Startup resistor (R_{str}) : The average of the minimum current supplied through the startup resistor is given by

$$I_{sup}^{avg} = \left(\frac{\sqrt{2} \cdot V_{line}^{min}}{\pi} - \frac{V_{start}}{2} \right) \cdot \frac{1}{R_{str}} \qquad (22)$$

where V_{line}^{min} is the minimum input voltage, V_{start} is the start voltage (15V) of FPS and R_{str} is the startup resistor. The startup resistor should be chosen so that I_{sup}^{avg} is larger than the maximum startup current (50uA). If not, Vcc can not be charged up to the start voltage and FPS will fail to start up.

The maximum startup time is determined as

$$T_{str}^{max} = C_e \cdot \frac{V_{start}}{(I_{sup}^{avg} - I_{start}^{max})} \qquad (23)$$

Where C_e is the effective Vcc capacitor (C_{a1}+C_{a2}) and I_{start}^{max} is the maximum startup current (50uA) of FPS.

Once the startup resistor (R_{str}) is determined, the maximum approximate power dissipation in R_{str} is obtained as

$$P_{str} = \frac{1}{R_{str}} \cdot \left(\frac{\left(V_{line}^{max}\right)^2 + V_{start}^2}{2} - \frac{2\sqrt{2} \cdot V_{start} \cdot V_{line}^{max}}{\pi} \right) \qquad (24)$$

where V_{line}^{max} is the maximum input voltage, which is specified in STEP-1. The startup resistor should have a proper dissipation rating based on the value of P_{str}.

[STEP-9] Determine the wire diameter for each winding based on the RMS current of each output.

The RMS current of the n-th secondary winding is obtained as

$$I_{sec(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1 - D_{max}}{D_{max}}} \cdot \frac{V_{RO} \cdot K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \qquad (25)$$

where D_{max} and I_{ds}^{rms} are specified in equations (6) and (9), $V_{o(n)}$ is the output voltage of the n-th output, $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage drop, V_{RO} is specified in STEP-3 and $K_{L(n)}$ is the load occupying factor for n-th output defined in equation (2).
The current density is typically 5A/mm^2 when the wire is long (>1m). When the wire is short with a small number of turns, a current density of 6-10 A/mm^2 is also acceptable. Avoid using wire with a diameter larger than 1 mm to avoid severe eddy current losses as well as to make winding easier. For high current output, it is recommended using parallel windings with multiple strands of thinner wire to minimize skin effect.

Check if the winding window area of the core, A_w (refer to Figure 6) is enough to accommodate the wires. The required winding window area (A_{wr}) is given by

$$A_{wr} = A_c / K_F \qquad (26)$$

where A_c is the actual conductor area and K_F is the fill factor. Typically the fill factor is 0.2~0.25 for single output applications and 0.15~0.2 for multiple outputs applications.
If the required window (A_{wr}) is larger than the actual window area (A_w), go back to the STEP-6 and change the core to a bigger one. Sometimes it is impossible to change the core due to cost or size constraints. In that case, reduce V_{RO} in STEP-3 or increase f_s^{min}, which reduces the primary side inductance (L_m) and the minimum number of turns for the primary (N_p^{min}) shown in equation (7) and (10).

[STEP-10] Choose the proper rectifier diodes in the secondary side based on the voltage and current ratings.

The maximum reverse voltage and the rms current of the rectifier diode ($D_{R(n)}$) of the n-th output are obtained as

$$V_{D(n)} = V_{o(n)} + \frac{V_{DC}^{max} \cdot (V_{o(n)} + V_{F(n)})}{V_{RO}} \qquad (27)$$

$$I_{D(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1 - D_{max}}{D_{max}}} \cdot \frac{V_{RO} K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \qquad (28)$$

where $K_{L(n)}$, V_{DC}^{max}, D_{max} and I_{ds}^{rms} are specified in equations (2), (4), (6) and (9), respectively, V_{RO} is specified in STEP-3, $V_{o(n)}$ is the output voltage of the n-th output and $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage drop. The typical

voltage and current margins for the rectifier diode are as follows

$$V_{RRM} > 1.3 \cdot V_{D(n)} \quad (29)$$

$$I_F > 1.5 \cdot I_{D(n)}^{rms} \quad (30)$$

where V_{RRM} is the maximum reverse voltage and I_F is the average forward current of the diode.

A quick selection guide for the Fairchild Semiconductor rectifier diodes is given in Table 3. In this table, t_{rr} is the maximum reverse recovery time.

Ultra Fast Recovery Diode				
Products	**V_{RRM}**	**I_F**	**t_{rr}**	**Package**
EGP10B	100 V	1 A	50 ns	DO-41
UF4002	100 V	1 A	50 ns	DO-41
EGP20B	100 V	2 A	50 ns	DO-15
EGP30B	100 V	3 A	50 ns	DO-210AD
FES16BT	100 V	16 A	35 ns	TO-220AC
EGP10C	150 V	1 A	50 ns	DO-41
EGP20C	150 V	2 A	50 ns	DO-15
EGP30C	150 V	3 A	50 ns	DO-210AD
FES16CT	150 V	16 A	35 ns	TO-220AC
EGP10D	200 V	1 A	50 ns	DO-41
UF4003	200 V	1 A	50 ns	DO-41
EGP20D	200 V	2 A	50 ns	DO-15
EGP30D	200 V	3 A	50 ns	DO-210AD
FES16DT	200 V	16 A	35 ns	TO-220AC
EGP10F	300 V	1 A	50 ns	DO-41
EGP20F	300 V	2 A	50 ns	DO-15
EGP30F	300 V	3 A	50 ns	DO-210AD
EGP10G	400 V	1 A	50 ns	DO-41
UF4004	400 V	1 A	50 ns	DO-41
EGP20G	400 V	2 A	50 ns	DO-15
EGP30G	400 V	3 A	50 ns	DO-210AD
UF4005	600 V	1 A	75 ns	DO-41
EGP10J	600 V	1A	75 ns	DO-41
EGP20J	600 V	2 A	75ns	DO-15
EGP30J	600 V	3 A	75 ns	DO-210AD
UF4006	800 V	1 A	75 ns	TO-41
UF4007	1000 V	1 A	75 ns	TO-41

Table 3. Fairchild Diode Quick Selection Table

[STEP-11] Determine the output capacitors considering the voltage and current ripple.

The ripple current of the n-th output capacitor ($C_{o(n)}$) is obtained as

$$I_{cap(n)}^{rms} = \sqrt{(I_{D(n)}^{rms})^2 - I_{o(n)}^2} \quad (31)$$

where $I_{o(n)}$ is the load current of the n-th output and $I_{D(n)}^{rms}$ is specified in equation (28). The ripple current should be smaller than the maximum ripple current specification of the capacitor. The voltage ripple on the n-th output is given by

$$\Delta V_{o(n)} = \frac{I_{o(n)} D_{max}}{C_{o(n)} f_s^{min}} + \frac{I_{ds}^{peak} V_{RO} R_{C(n)} K_{L(n)}}{(V_{o(n)} + V_{F(n)})} \quad (32)$$

where $C_{o(n)}$ is the capacitance, $R_{c(n)}$ is the effective series resistance (ESR) of the n-th output capacitor, $K_{L(n)}$, D_{max} and I_{ds}^{peak} are specified in equations (2), (6) and (8) respectively, V_{RO} is specified in STEP-3, $I_{o(n)}$ and $V_{o(n)}$ are the load current and output voltage of the n-th output, respectively and $V_{F(n)}$ is the diode ($D_{R(n)}$) forward voltage drop.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. In those cases, use additional LC filter stages (post filter) to reduce the ripple on the output.

[STEP-12] Design the synchronization network.

The FSCQ-series employs a quasi-resonant switching technique to minimize the switching noise and loss. In this technique, a capacitor (C_r) is added between the MOSFET drain and source as shown in Figure 12. The basic waveforms of a Quasi-Resonant Converter are shown in Figure 13. The external capacitor lowers the rising slope of drain voltage, which reduces the EMI caused by the MOSFET turn-off. To minimize the MOSFET switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value as shown in Figure 13.

The optimum MOSFET turn-on time is indirectly detected by monitoring the Vcc winding voltage as shown in Figure 12 and 13. The output of the sync detect comparator (CO) becomes high when the sync voltage (V_{sync}) exceeds 4.6V and low when the V_{sync} reduces below 2.6V. The MOSFET is turned on at the falling edge of the sync detect comparator output (CO).

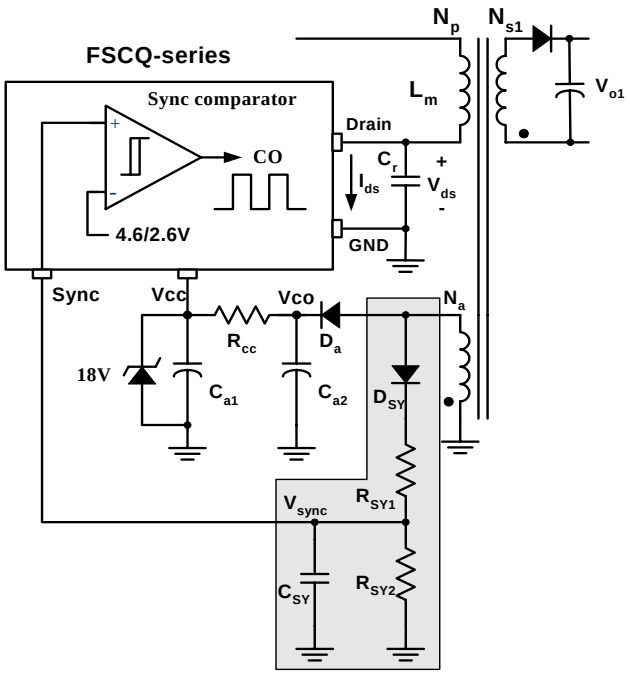


Figure. 12 Synchronization Circuit

The peak value of the sync signal is determined by the voltage divider network R_{SY1} and R_{SY2} as

$$V_{sync}^{pk} = \frac{R_{SY2}}{R_{SY1} + R_{SY2}} \cdot V_a^{normal} \qquad (33)$$

where V_a^{normal} is the Vcc auxiliary voltage in normal mode.

Choose the voltage divider R_{SY1} and R_{SY2} so that the peak value of sync voltage (V_{sync}^{pk}) is lower than the OVP threshold voltage (12V) to avoid triggering OVP in normal operation. It is typical to set V_{sync}^{pk} to be 8~10V.

To synchronize the V_{sync} with the MOSFET drain voltage, the sync capacitor (C_{SY}) should be chosen so that T_F is same as T_Q as shown in Figure 13. T_F and T_Q are given as

$$T_F = \pi \cdot \sqrt{L_m \cdot C_{eo}} \qquad (34)$$

$$T_Q = R_{SY2} \cdot C_{SY} \cdot ln\left(\frac{V_a^{normal}}{2.6} \cdot \frac{R_{SY2}}{R_{SY1} + R_{SY2}}\right) \qquad (35)$$

where L_m is the primary side inductance of the transformer, N_s and N_a are the number of turns for the output winding and Vcc winding, respectively, V_a^{normal} is the Vcc auxiliary voltage in normal mode and C_{eo} is the effective MOSFET output capacitance (C_{oss}+C_r).

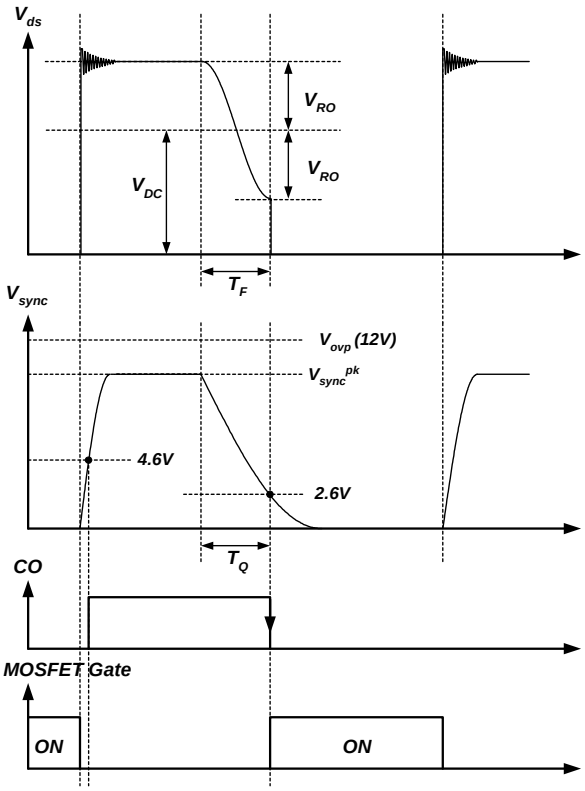


Figure. 13 Synchronization Waveforms

[STEP-13] Design voltage drop circuit for the burst operation.

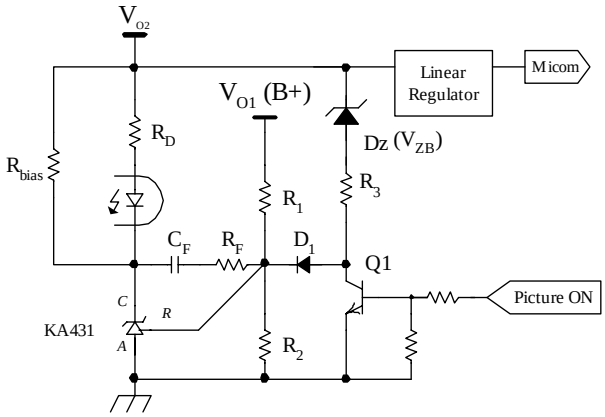


Figure 14. Typical Feedback Circuit to Drop Output Voltage in Standby Mode

To minimize the power consumption in the standby mode, FSCQ-series employs burst operation. Once FPS enters into burst mode, all output voltages and effective switching frequencies are reduced. Figure 14 shows the typical output voltage drop circuit for C-TV applications. Under normal

operation, the picture on signal is applied and the transistor Q_1 is turned on, which de-couples R_3, D_z and D_1 from the feedback network. Thus, only V_{o1} is regulated by the feedback circuit in normal operation and is determined as

$$V_{o1} = 2.5 \cdot \left(\frac{R_1 + R_2}{R_2}\right) \quad (36)$$

Figure 15 shows the standby mode operation waveforms. In standby mode, the picture on signal is disabled and the transistor Q_1 is turned off, which couples R_3, D_z and D_1 to the reference pin of KA431. If R_3 is much smaller than R_1, V_{o2} is dominant in the feedback loop. Before V_{o2} drops to V_{o2}^{stby}, the voltage on the reference pin of KA431 is higher than 2.5V, which increases the current through the opto LED. This pulls down the feedback voltage (V_{FB}) of FPS and forces to stop switching. Once FPS stops switching, V_{o2} decrease, and when V_{o2} reaches V_{o2}^{stby}, the current through the opto LED decreases allowing the feedback voltage to rise. When the feedback voltage reaches 0.4V, FPS resumes switching with a predetermined peak drain current. Assuming that the forward voltage drop of D_1 is 0.5V, the approximate output voltage for V_{o2} in standby mode is given by

$$V_{02}^{stby} = V_{ZB} + 0.5 + 2.5 \quad (37)$$

where V_{ZB} is the zener breakdown voltage of D_z.

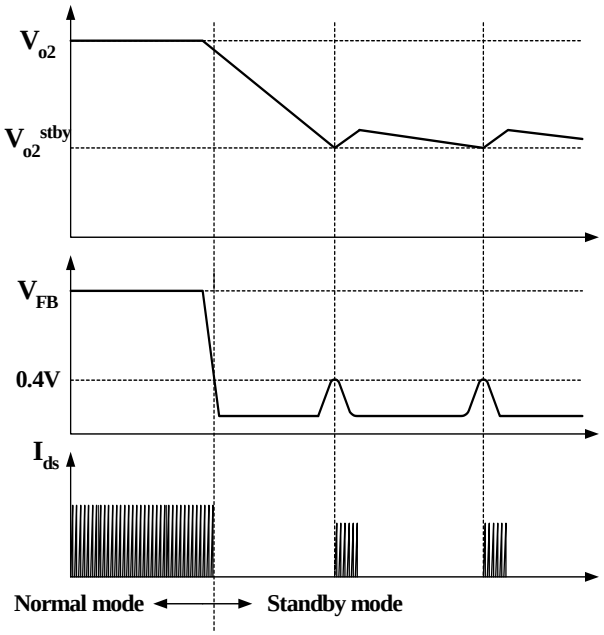


Figure 15. Burst Operation Waveforms

[STEP-14] Design the feedback control circuit.

Since FSCQ-series employs current mode control as shown in Figure 16, the feedback loop can be easily implemented with a one-pole and one-zero compensation circuit. The current control factor of FPS, K is defined as

$$K = \frac{I_{pk}}{V_{FB}} = \frac{I_{LIM}}{V_{FBsat}} \quad (38)$$

where I_{pk} is the peak drain current and V_{FB} is the feedback voltage for a given operating condition, I_{LIM} is the current limit of the FPS and V_{FBsat} is the internal feedback saturation voltage, which is typically 2.5V.

In order to express the small signal AC transfer functions, the small signal variations of feedback voltage (v_{FB}) and controlled output voltage (v_{o1}) are introduced as $\hat{v}_{FB}$ *and* $\hat{v}_{o1}$.

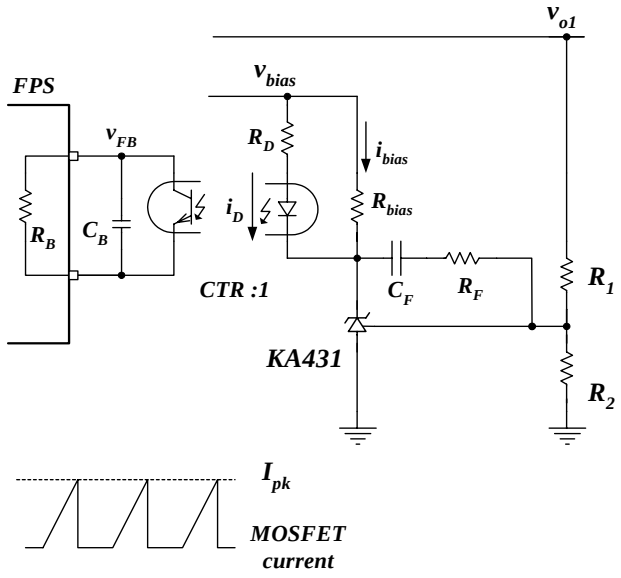


Figure 16. Control Block Diagram

For quasi-resonant flyback converter, the control-to-output transfer function using current mode control is given by

$$G_{vc} = \frac{\hat{v}_{o1}}{\hat{v}_{FB}} = \frac{K \cdot R_L V_{DC}(N_p/N_{s1})}{2(2V_{RO} + v_{DC})} \cdot \frac{(1 + s/w_z)(1 - s/w_{rz})}{1 + s/w_p} \quad (39)$$

where V_{DC} is the DC input voltage, R_L is the effective total load resistance of the controlled output, which is defined as V_{o1}^2/P_o , N_p and N_{s1} are specified in STEP-7, V_{RO} is specified in STEP-3, V_{o1} is the reference output voltage, P_o is specified in STEP-1 and K is specified in equation (38). The pole and zeros of equation (39) are defined as

$$w_z = \frac{1}{R_{c1}C_{o1}},\ w_{rz} = \frac{R_L(1-D)^2}{DL_m(N_{s1}/N_p)^2} \ \text{ and } \ w_p = \frac{(1+D)}{R_L C_{o1}}$$

where L_m is specified in equation (7), D is the duty cycle of

the FPS, C_{o1} is the output capacitor of V_{o1} and R_{C1} is the ESR of C_{o1}.

When the converter has more than one output, the low frequency control-to-output transfer function is proportional to the parallel combination of all load resistance, adjusted by the square of the turns ratio. Therefore, the effective load resistance is used in equation (39) instead of the actual load resistance of V_{o1}. Notice that there is a right half plane (RHP) zero (w_{rz}) in the control-to-output transfer function of equation (39). Because the RHP zero reduces the phase by 90 degrees, the crossover frequency should be placed below the RHP zero.

Figure 17 shows the variation of a quasi-resonant flyback converter control-to-output transfer function for different input voltages. This figure shows the system poles and zeros together with the DC gain change for different input voltages. The gain is highest at the high input voltage condition and the RHP zero is lowest at the low input voltage condition.

Figure 18 shows the variation of a quasi-resonant flyback converter control-to-output transfer function for different loads. This figure shows that the gain between f_p and f_z does not change for different loads and the RHP zero is lowest at the full load condition.

The feedback compensation network transfer function of Figure 16 is obtained as

$$\frac{\hat{v}_{FB}}{\hat{v}_{o1}} = -\frac{w_i}{s} \cdot \frac{1 + s/w_{zc}}{1 + s/w_{pc}} \qquad (40)$$

$$\text{where } w_i = \frac{R_B \cdot CTR}{R_1 R_D C_F},\ w_{zc} = \frac{1}{R_F C_F},\ w_{pc} = \frac{1}{R_B C_B}$$

and R_B is the internal feedback bias resistor of FPS, which is typically 2.8kΩ, CTR is the current transfer ratio of opto coupler and R_1, R_D, R_F, C_F and C_B are shown in Figure 16.

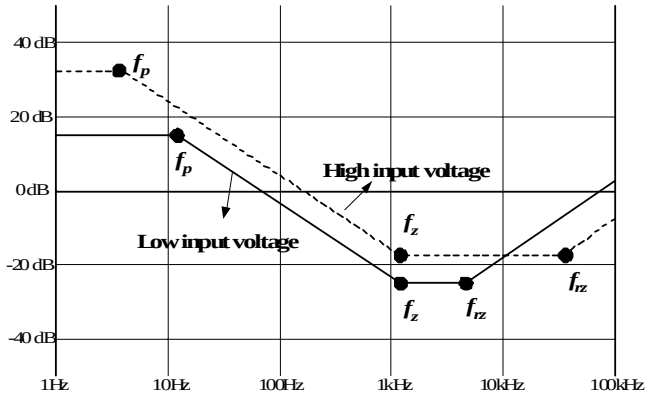


Figure 17. QR Flyback Converter Control to Output Transfer Function Variation for Different Input Voltages

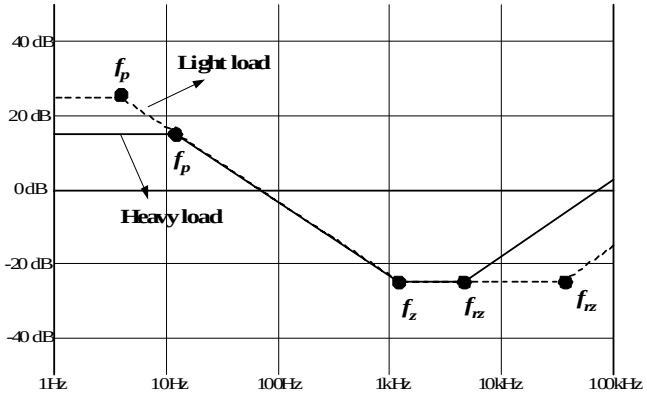


Figure 18. QR Flyback Converter Contro to Output Transfer Function Variation for Different Loads

When the input voltage and the load current vary over a wide range, determining the worst case for the feedback loop design is difficult. The gain together with zeros and poles varies according to the operating conditions.

One simple and practical solution to this problem is designing the feedback loop for low input voltage and full load condition with enough phase and gain margin. The RHP zero is lowest at low input voltage and full load condition. The gain increases only about 6dB as the operating condition is changed from the lowest input voltage to the highest input voltage condition under universal input condition.

The procedure to design the feedback loop is as follows

(a) Set the crossover frequency (f_c) below 1/3 of RHP zero to minimize the effect of the RHP zero. Set the crossover frequency below half of the minimum switching frequency (f_s^{min}).

(b) Determine the DC gain of the compensator (w_i/w_{zc}) to cancel the control-to-output gain at f_c.

(c) Place a compensator zero (f_{zc}) around $f_c/3$.

(d) Place a compensator pole (f_{pc}) around $3f_c$.

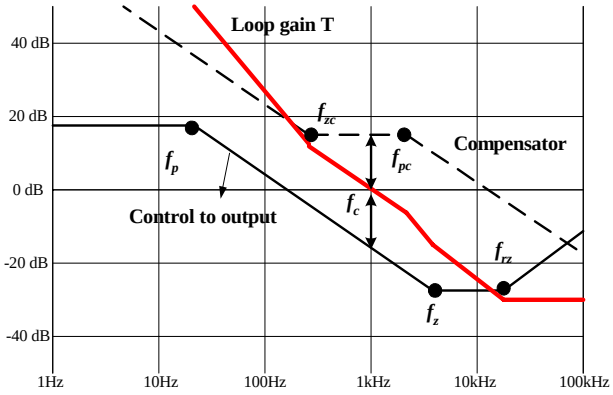


Figure 19. Compensator Design

When determining the feedback circuit component, there are some restrictions as described below:

(a) Design the voltage divider network of R_1 and R_2 to provide 2.5V to the reference pin of the KA431. The relationship between R_1 and R_2 is given as

$$R_2 = \frac{2.5 \cdot R_1}{V_{o1} - 2.5} \quad (41)$$

where V_{o1} is the reference output voltage.

(b) The capacitor connected to feedback pin (C_B) is related to the shutdown delay time in an overload condition by

$$T_{delay} = (V_{SD} - 2.5) \cdot C_B / I_{delay} \quad (42)$$

where V_{SD} is the shutdown feedback voltage and I_{delay} is the shutdown delay current. Typical values for V_{SD} and I_{delay} are 7.5V and 5uA, respectively. In general, a 20 ~ 50 ms delay is typical for most applications. Because C_B also determines the high frequency pole (w_{pc}) of the compensator transfer function as shown in equation (40), too large a C_B can limit the control bandwidth by placing w_{pc} at too low a frequency. Typical value for C_B is 10-50nF.

(c) The resistors R_{bias} and R_D used together with the opto-coupler H11A817A and the shunt regulator KA431 should be designed to provide proper operating current for the KA431 and to guarantee the full swing of the feedback voltage for the FPS device chosen. In general, the minimum cathode voltage and current for the KA431 are 2.5V and 1mA, respectively. Therefore, R_{bias} and R_D should be designed to satisfy the following conditions.

$$\frac{V_{bias} - V_{OP} - 2.5}{R_D} > I_{FB} \quad (43)$$

$$\frac{V_{OP}}{R_{bias}} > 1mA \quad (44)$$

where V_{bias} is the KA431 bias voltage as shown in Figure 16 and V_{OP} is opto-diode forward voltage drop, which is typically 1V. I_{FB} is the feedback current of FPS, which is typically 1mA.

3. Design Example Using FPS Design Assistant

Application	Device	Input Voltage	Output Power	Output Voltage (Rated Current)	Ripple Spec
Color TV	FSCQ0765RT	85-265Vac (60Hz)	83W	125V (0.4A) 24V (0.5A) 18V (0.5A) 12V (1.0A)	±5% ±5% ±5% ±5%

FAIRCHILD SEMICONDUCTOR™

FPS Design Assistant for AN4146

Ver 1.00 ***by H.S. Choi***

Blue cells are the input parameters

Red cells are the output parameters

1. Define the system specifications

Minimum Line voltage (V_{line}^{min})	85	V.rms
Maximum Line voltage (V_{line}^{max})	265	V.rms
Line frequency (f_L)	60	Hz

	$V_{o(n)}$		$I_{o(n)}$		$P_{o(n)}$		$K_{L(n)}$	
1st output (Vo1) ; regulated by feedback	125	V	0.40	A	50	W	60	%
2nd output (Vo2)	24	V	0.50	A	12	W	14	%
3rd output (Vo3)	18	V	0.50	A	9	W	11	%
4th output (Vo4)	12	V	1.00	A	12	W	14	%
5th output (Vo5)		V		A	0	W	0	%

Maximum output power (P_o) =	83.0	W
Estimated efficiency (E_{ff})	82	%
Maximum input power (P_{in}) =	101.2	W

- It is assumed that the efficiency is 83% at the minimum input voltage and full load condition.

2. Determine DC link capacitor and DC link voltage range

DC link capacitor (C_{DC})	220	uF
Minimum DC link voltage (V_{DC}^{min}) =	91	V
Maximum DC link voltage (V_{DC}^{max})=	375	V

- Since the maximum input power is 101.2W, the DC link capacitor is set to be 220uF by 2uF/Watt.

3. Determine the reflected output (V_{RO})

Output voltage reflected to primary (V_{RO})	126	V
Maximum nominal Drain voltage (V_{ds}^{nom}) =	501	V

- V_{RO} is set to be 126V so that V_{ds}^{nom} should be about 77% of BV_{dss}

4. Determine transformer primary side inductance (Lm)

Drain voltage falling time (T_F)	2.3	us
Minimum Switching frequency of FPS (f_{s_min})	24	kHz
Maximum duty cycle (D_{max}) =	0.55	
Primary side inductance (L_m) =	514	uH
Maximum peak drain current (I_{ds}^{peak}) =	4.05	A
RMS drain current (I_{ds}^{rms}) =	1.73	A

5. Choose the proper FPS considering the input power and current limit

Typical current limit of FPS (I_{LIM})	5.00	A		
Minimum I_{LIM} considering tolerance	4.40	A	>	4.05 A
	->O.K.			

- Considering the tolerance of 12%, FSCQ0765RT is chosen, whose pulse-by-pulse current limit is 5A (typical).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Peak Current Limit (Note3)	I_{LIM}	-	4.4	5.0	5.6	A

6. Determine the proper core and the minimum primary turns

Maximum flux density swing in normal mode (Δ	0.30	T	-->	N_p> 63.69 T
Maximum flux density in transient (B_{sat})	0.38	T	-->	N_p> 62.07 T
Cross sectional area of core (A_e)	109	mm^2		
Minimum primary turns (N_p^{min})=	63.7	T		

- EER3540 core is chosen, whose cross sectional area is 109mm^2.

7. Determine the number of turns for each output and Vcc drop circuit

Vo2 in standby mode (V_{o2}^{stby})	8.0	V	V_{o2}= 24 V in normal mode		
Vcc auxiliary voltage drop ratio (K_{drop}) =	0.37				
Minimum V_a in standby mode (V_a^{stby})	13.0	V			
V_a in normal mode (V_a^{normal}) =	37.7	V			

	$V_{F(n)}$				# of turns	
Winding for Va (37.7V)	1.2	V	19.7	=>	20	T
Winding for Vo1 (125V)	1.2	V	64	=>	64	T
Winding for Vo2 (24V)	1.2	V	12.8	=>	13	T
Winding for Vo3 (18V)	1.2	V	9.7	=>	10	T
Winding for Vo4 (12V)	1.2	V	6.7	=>	7	T
Winding for Vo5 (V)		V	0.0	=>	0	T
Number of turns for primary winding (N_p)=	64	T	> 63.7 T			
	---->enough turns					
Ungapped AL value (AL)	3130	nH/T^2				
Gap length (G) ; center pole gap =	1.04337	mm				

Maximum operating current of FPS (I_{op})	6	mA				
MOSFET input capacitance (C_{iss})	1840	pF				
Breakdown voltage of Vcc zener diode	18	V				
Current consummed by FPS (Icc) =	9.0	mA		at	90	kHz
Vcc drop resistor (Rcc)	1.5	kΩ	<		2	kΩ
Power dissipation of Rcc =	0.3	W				

- In standby mode, V_{o2} is reduced from 24V to 8V. In order to prevent Vcc under voltage lockout in standby mode, V_a in standby mode is designed as 13V. Then, V_a would be 37.7V in normal mode.

-Assuming that the maximum switching frequency is 90kHz, the maximum current consumed by FPS is 9mA. Vcc resistor is determined as 1.5kΩ.

8. Determine the startup resistor

Maximum Startup current of FPS (I_{start})	50	uA				
Startup resistor	240	kΩ	<		616	kΩ
Effective Vcc capacitor (Ce)	20	uF				
Maximum dissipation in startup resistor =	0.13	W		at	265	Vac
Maximum startup time (T_{str}^{max}) =	3.83	s		at	85	Vac

9. Determine the wire diameter for each winding

	Diameter			Parallel	$I_{D(n)}^{rms}$		(A/mm^2)
Primary winding	0.6	mm	×	1	1.7	A	6.1
Winding for Vcc (37.7V)	0.3	mm	×	1	0.1	A	1.4
Winding for Vo1 (125V / 0.4A)	0.5	mm	×	1	0.9	A	4.8
Winding for Vo2 (24V / 0.5A)	0.4	mm	×	2	1.1	A	4.5
Winding for Vo3 (18V / 0.5A)	0.4	mm	×	2	1.1	A	4.5
Winding for Vo4 (12V / 1A)	0.5	mm	×	2	2.2	A	5.5
Winding for Vo5 (V / A)		mm	×		#####	A	####

Copper area (A_c) =	40.56	mm^2
Fill factor (K_F)	0.2	
Required window area (A_w)	202.78	mm^2

- For each winding, the diameter of wire is determined so that the current density should be about 5A/mm^2
- For EER3540 core, the winding window area is 223mm^2. Assuming a fill factor of 0.2, this core is enough to accommodate the wires.

10. Choose the rectifier diode in the secondary side

	$V_{D(n)}$		$I_{D(n)}^{rms}$	
Rectifier diode for Vcc	153	V	0.10	A
Rectifier diode for Vo1 (125V / 0.4A)	500	V	0.95	A
Rectifier diode for Vo2 (24V / 0.5A)	99	V	1.14	A
Rectifier diode for Vo3 (18V /0.5A)	75	V	1.12	A
Rectifier diode for Vo1 (12V /1A)	51	V	2.17	A
Rectifier diode for Vo5 (V /A)	0	V	#####	A

Vcc winding	1N4937	Ultra fast recovery
Vo1 (125V)	EGP20J (600V/2A)	Ultra fast recovery
Vo2 (24V)	EGP20D (200V/2A)	Ultra fast recovery
Vo3 (18V)	EGP20D (200V/2A)	Ultra fast recovery
Vo4 (12V)	EGP20D (200V/2A)	Ultra fast recovery

11. Determine the output capacitor

	$C_{o(n)}$		$R_{C(n)}$		$I_{cap(n)}$		$\Delta V_{o(n)}$	
Output capacitor for Vo1 (125V / 0.4A)	100	uF	100	mΩ	0.9	A	0.3	V
Output capacitor for Vo2 (24V / 0.5A)	1000	uF	100	mΩ	1.0	A	0.3	V
Output capacitor for Vo3 (18V / 0.5A)	1000	uF	100	mΩ	1.0	A	0.3	V
Output capacitor for Vo4 (12V / 1A)	1000	uF	100	mΩ	1.9	A	0.6	V
Output capacitor for Vo5 (V / A)		uF		mΩ	#####	A	####	V

12. Design the synchronization network

Peak value of Sync voltage (V_{sync}^{pk})	9.0	V	$4.6 < V_{sync}^{pk} < 12V$ (V_{OVP})
Sync voltage divider resistor (R_{sy1})	1500	Ω	
Sync voltage divider resistor (R_{sy2})	470	Ω	
Effective output capacitance of MOSFET	1.0	nF	(Coss + Cr)
Sync capacitor (C_{sy})	3.9	nF	

- Since the output capacitance of MOSFET is 100pF (typical), external capacitor (Cr) of 1nF is used.

13. Design voltage drop circuit for the burst operation

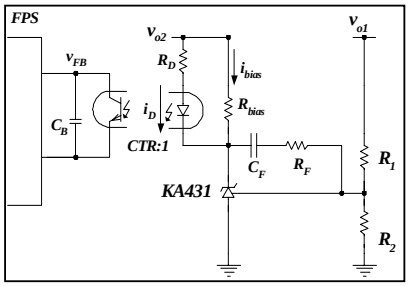
Vo2 in standby mode (V_{o2}^{stby})	8.0	V
Breakdown voltage of zener diode, Dz	5.0	V

- Zener diode with a breakdown voltage of 5.1V is chosen.

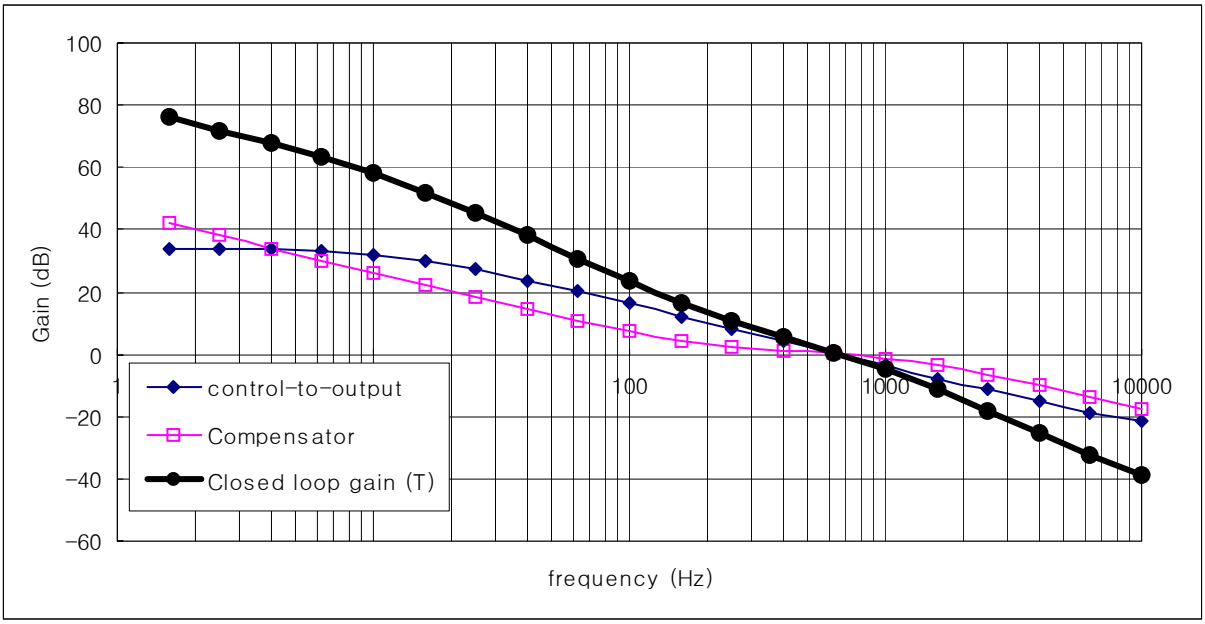
14. Design the feedback control circuit

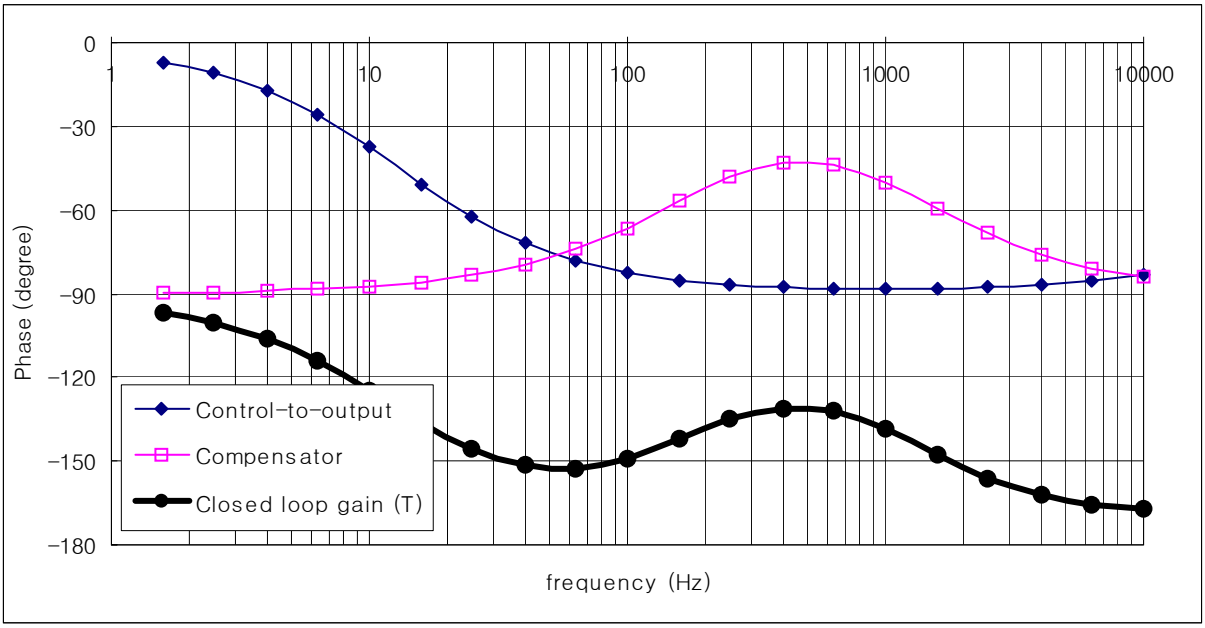
Control-to-output DC gain =	50				
Control-to-output zero (w_z) =	100.0	krad/s =>	f_z=	15,924	Hz
Control-to-output RHP zero (w_{rz})=	136.0	krad/s =>	f_{rz}=	21,650	Hz
Control-to-output pole (w_p)=	82	rad/s =>	f_p=	13	Hz

Voltage divider resistor (R_1)	100	kΩ
Voltage divider resistor (R_2)=	2.0	kΩ
Opto coupler diode resistor (R_D)	1	kΩ
KA431 Bias resistor (R_{bias})	1.2	kΩ
Feeback pin capacitor (C_B) =	47	nF
Feedback Capacitor (C_F) =	22	nF
Feedback resistor (R_F) =	39	kΩ
Current transfer ratio of opto coupler (CTR)	100	%



Feedback integrator gain (w_i) =	1273	rad/s =>	f_i=	203	Hz
Compensator zero (w_{zc})=	1166	rad/s =>	f_{zc}=	186	Hz
Compensator pole (w_{pc})=	7599	rad/s =>	f_{pc}=	1,210	Hz





- The control bandwidth (crossover frequency) is about 600Hz with a phase margin of 50 degrees.

Design Summary

- High efficiency (>80% at 85Vac input)
- Wider load range through the extended quasi-resonant operation
- Low standby mode power consumption (<1W)
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (20ms)

Key Design Notes

- 24V output is designed to drop to around 8V in standby mode
- Zener diode ZD102 is used for a safety test such as UL. When the drain pin and feedback pin are shorted, the zener diode fails and remains short, which causes the fuse (F1) to pop and prevents explosion of the opto-coupler (IC301). This zener diode also increases the immunity against line surge.

1. Schematic

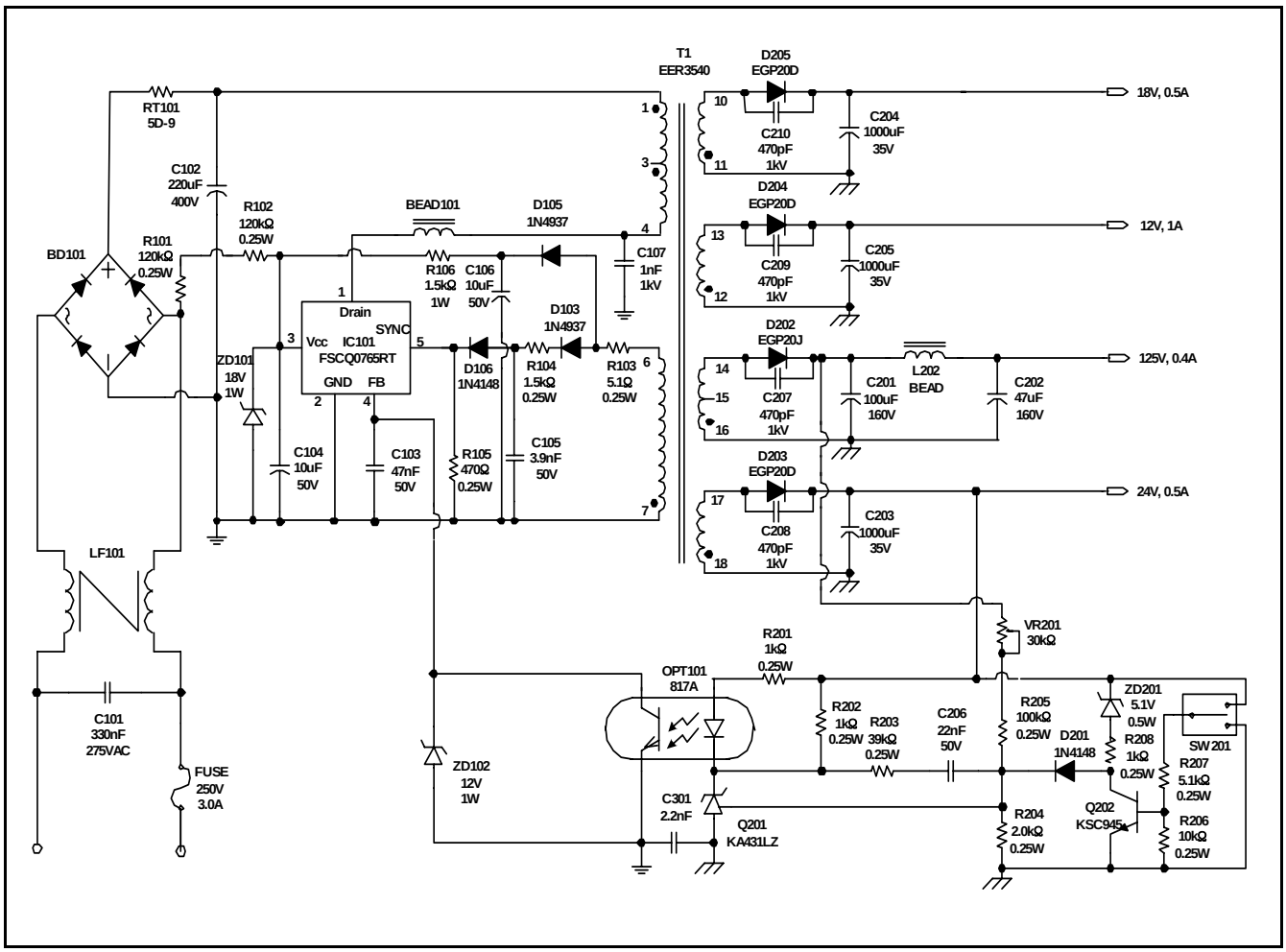


Figure 20. Schematic of Design Example

2. Transformer Specifications

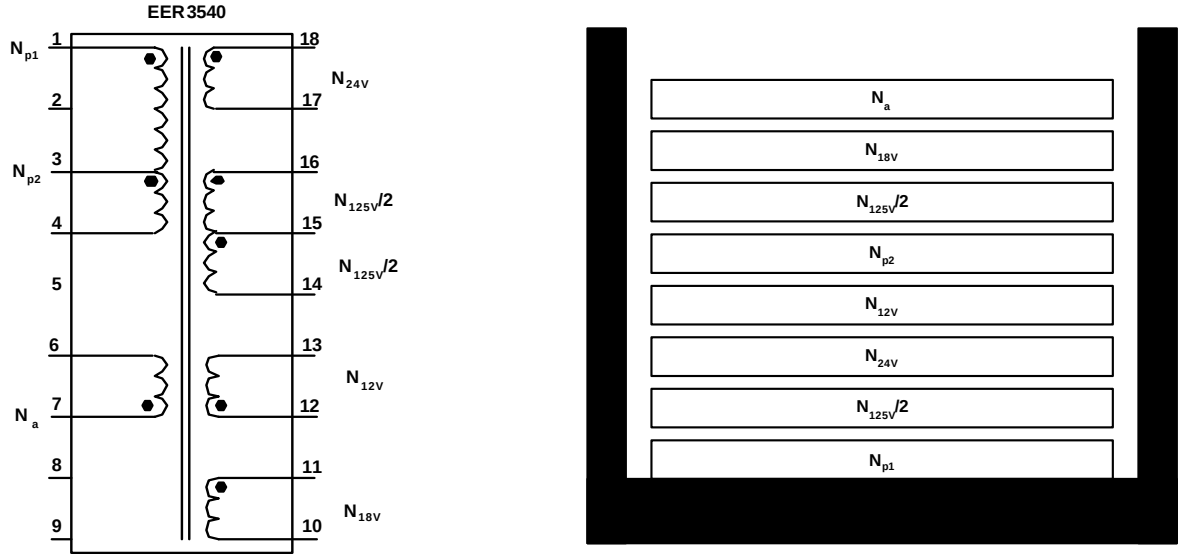


Figure 21. Transformer Schematic Diagram

Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
N_{p1}	1 - 3	$0.6^{\phi} \times 1$	32	Center Winding
$N_{125V/2}$	16 - 15	$0.5^{\phi} \times 1$	32	Center Winding
N_{24V}	18 - 17	$0.4^{\phi} \times 2$	13	Center Winding
N_{12V}	12 - 13	$0.5^{\phi} \times 2$	7	Center Winding
N_{p2}	3 - 4	$0.6^{\phi} \times 1$	32	Center Winding
$N_{125V/2}$	15 - 14	$0.5^{\phi} \times 1$	32	Center Winding
N_{18V}	11 - 10	$0.4^{\phi} \times 2$	10	Center Winding
N_a	7 - 6	$0.3^{\phi} \times 1$	20	Center Winding

Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	514uH ± 5%	1kHz, 1V
Leakage Inductance	1 - 3	10uH Max	2^{nd} all short

Core & Bobbin
Core : EER 3540
Bobbin : EER3540
Ae : 109 mm^2

Experimental Verification

To show the validity of the design procedure presented in this application note, we have built and tested the converter in the design example. All the circuit components are used as designed in the design example. The schematic and transformer specifications are shown in Figure 20 and 21, respectively.

The Figure 22 shows the FPS drain current and the DC link voltage waveforms at the minimum input voltage and full load condition. As shown, the minimum DC link voltage (V_{DC}^{min}) is about 90V, which is the same as the designed value in STEP-2 of page 13.

Figure 23 shows the FPS drain current and voltage waveforms at the minimum input voltage and full load condition. As can be seen, the maximum peak drain current (I_{ds}^{peak}) is about 3.9A and the minimum switching frequency (f_s^{min}) is 26kHz. The values in the design are 4.05A for I_{ds}^{peak} and 24kHz for f_s^{min} as can be seen in STEP-4 of page 14.

Figure 24 shows the FPS drain current and voltage waveforms at the maximum input voltage and full load condition. As calculated in STEP-3 of page 13, the nominal drain voltage is about 500V.

Figures 25 and 26 show the waveforms of Vsync, drain voltage and drain current at the maximum input voltage and full load condition. As designed, the MOSFET drain fall time is 2.3us and the MOSFET is turned on when the drain voltage reaches its minimum value.

Figure 27 shows the waveforms of Vcc, drain voltage and drain current. The measured startup time is 2.45s, which is smaller than the calculated maximum startup time of 3.83s in STEP-8 of page 15. When the typical value for the startup current (25us) is used for the equation (19), the typical startup time is calculated as

$$T_{str}^{max} = C_e \cdot \frac{V_{start}}{(I_{sup}^{avg} - I_{start}^{max})} = 2.91s$$

Figure 28 shows the output voltage drop in standby mode. As designed, the 24V output drops down to 8V. Figure 29 shows the detailed burst mode operation waveforms. Burst mode operation alternately enables and disables switching of the MOSFET thereby reducing switching loss in standby mode.

The Table 4 shows the line regulation of each output.

The Figure 30 shows the measured efficiency at the full load condition for different input voltages. The minimum efficiency is about 81% at the minimum input voltage condition.

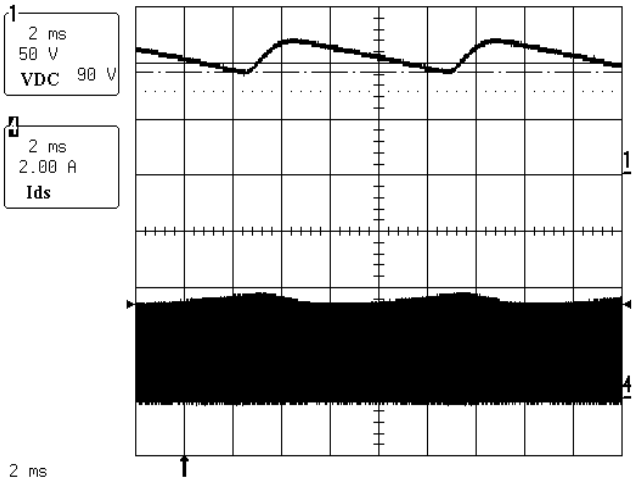


Figure 22. Waveforms of Drain Current and DC Link Voltage at 85Vac and Full load Condition (Time:2ms/div)

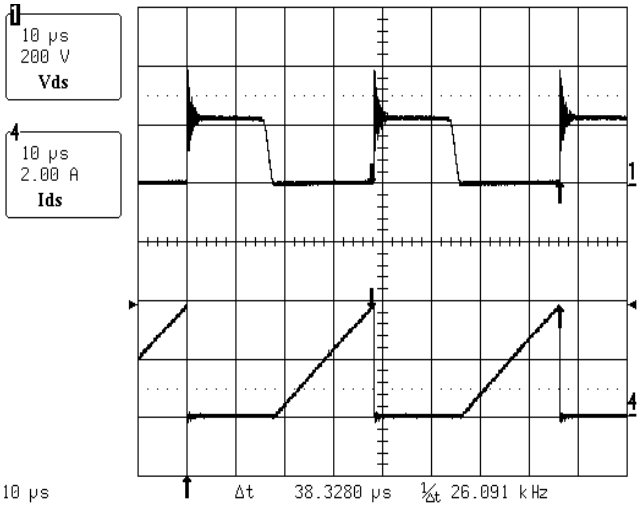


Figure 23. Waveforms of Drain Current and Voltage at 85Vac and Full Load Condition (Time : 10us/div)

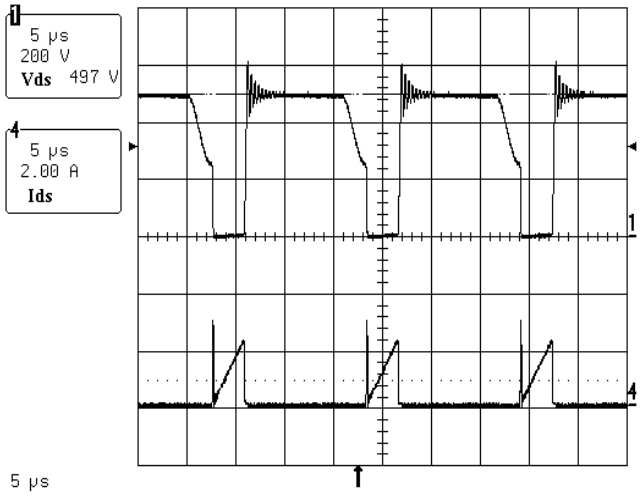


Figure 24. Waveforms of Drain Current and Voltage at 265Vac and Full Load Condition (Time : 5us/div)

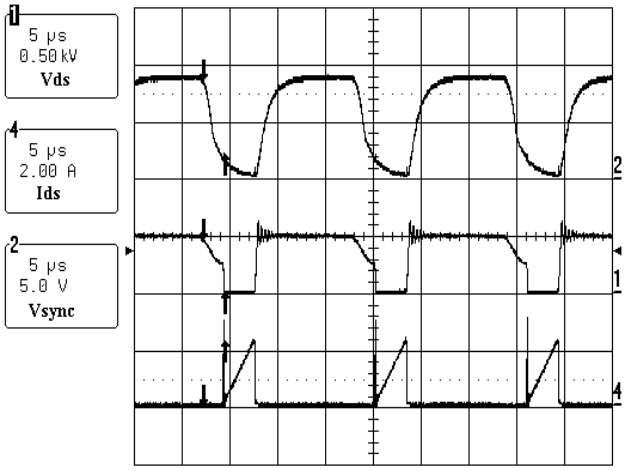


Figure 25. Vsync, Vds and Ids Waveforms at 265Vac and Full Load Condition (Time : 5us/div)

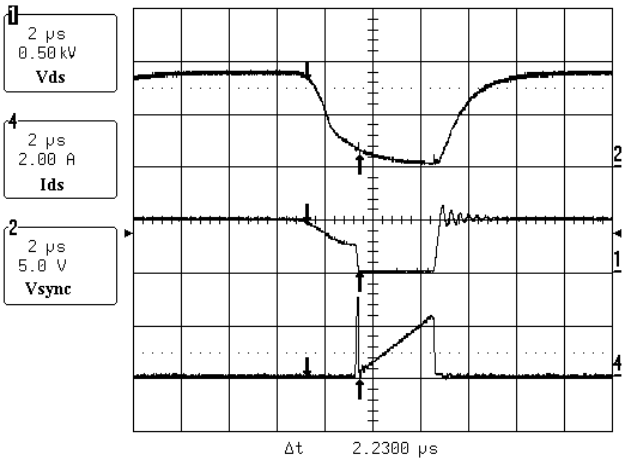


Figure 26. Vsync, Vds and Ids Waveforms at 265Vac and Full Load Condition (Time : 2us/div)

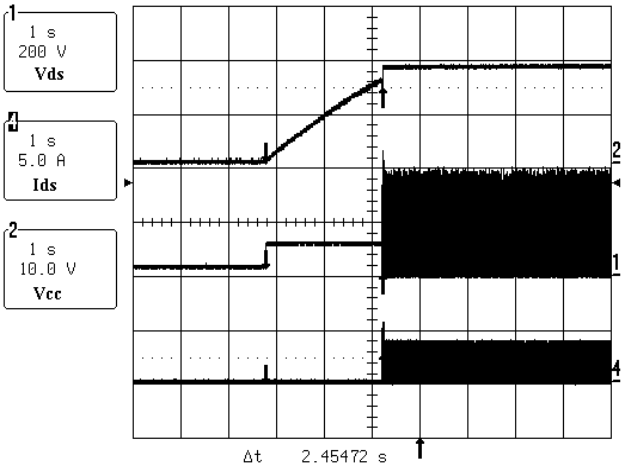


Figure 27. Vcc, Vds and Ids Waveforms at 265Vac and Full Load Condition (Time : 2/div)

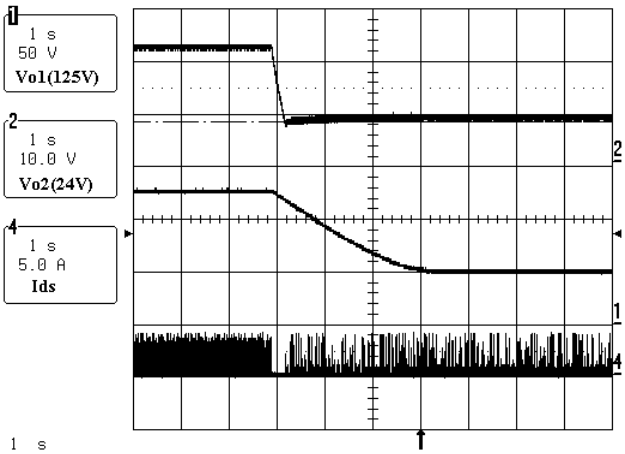


Figure 28. Output Voltage Drop in the Standby Mode

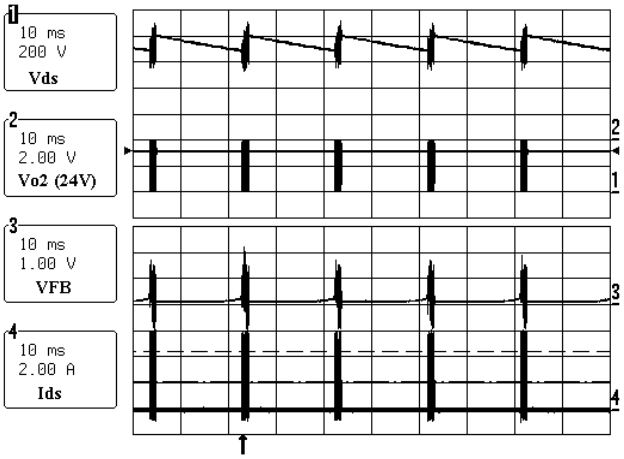


Figure 29. Burst Mode Operation

Input voltage	V_{o1}(125V)	V_{o2} (24)	V_{o3} (18V)	V_{o4} (12V)
85Vac	**125.3 V**	**24.25 V**	**18.88 V**	**12.85 V**
110Vac	**125.3 V**	**24.23 V**	**18.87 V**	**12.84V**
160Vac	**125.3 V**	**24.20 V**	**18.87 V**	**12.82 V**
220Vac	**125.3V**	**24.19 V**	**18.85 V**	**12.81 V**
265Vac	**125.3 V**	**24.18 V**	**18.85 V**	**12.79 V**

Table 4. Line Regulation of Each Output at Full Load Condition

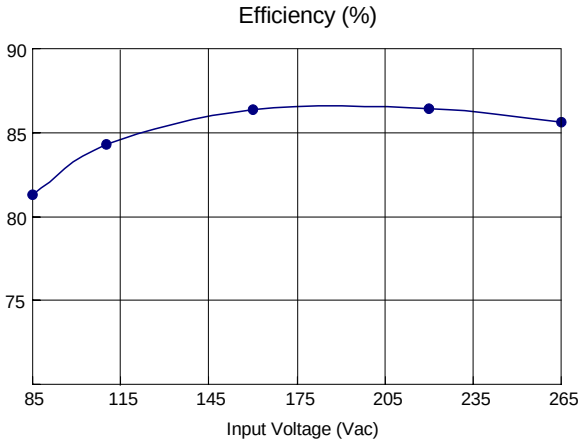


Figure 30. Measured Efficiency

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