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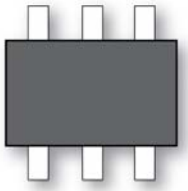
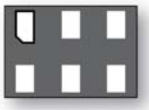
AN-8030
MicroPak2™ Package Applications Guide

Introduction

Fairchild Semiconductor is a global supplier of high-performance semiconductors, offering products used in a wide range of applications (mobile phones, PDAs, etc). Fairchild's Signal Path and TinyLogic® family consists of a broad spectrum of MicroPak™ packages with either 6 or 8 leads *(see Table 1)*. The MicroPak2™ package is Fairchild's latest addition to the family. With 1mm × 1mm body size and 0.35mm pitch, this package is a smaller version of the MicroPak 6 package.

This applications guide provides some general guidelines for developing land pattern designs, stencil design, and board-level assembly processes for the MicroPak2™ package. These guidelines are very general in nature and, since manufacturing practices and end-use applications vary, they should be used as starting points to further optimize designs and processes for specific manufacturing practices.

Table 1. Package Comparison

Fairchild Offers a Variety of Industry Leading Packages			
Package Migration Comparison and Options			
Measurements (mm)	**SC70-6**	**MicroPak-6**	**MicroPak2**
Mounted Width	2.10	1.00	1.0
Body Width	1.25	1.00	1.0
Length	2.00	1.45	1.0
Height	0.90	0.55	0.55
Pin Pitch	0.65	0.50	0.35

Application Board Design

Land Pattern Design

Two land pattern designs are recommended for the MicroPak2 package. The first is a Universal Pad Design which is to be used when board space availability is not a constraining factor in board design. The second design, the Space Constrained Design, is recommended for those applications where board space is limited. The dimensions for both types of pad designs are shown in Figure 1.

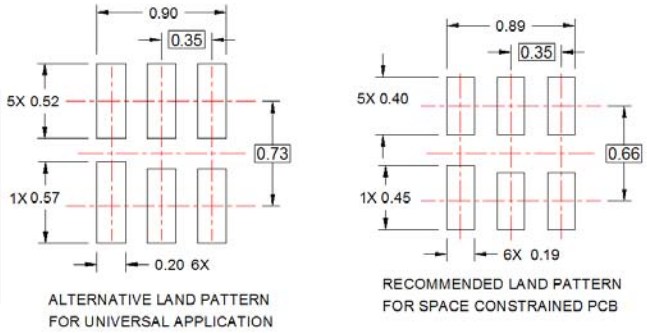


Figure 1. Schematic of Dimensions of Pad Designs

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Solder Paste Stencil Printing and Assembly Process

Stencil Design

Stencil design is instrumental in determining the quality of a solder joint by controlling the amount of solder paste deposited on the substrate land patterns. For the MicroPak2™ package, stencil aperture size-to-land size ratios of 1:1, 0.95:1, and 0.9:1 were investigated for the two recommended land pattern designs; space-constrained land pattern design and universal land pattern design. For a 0.004" stencil, the area ratios for the different-sized apertures range from 0.57 to 0.73. The area ratio of the stencil apertures is a primary factor in determining how well any particular stencil prints solder paste. Area ratio is the ratio between the open area of the stencil aperture and the area of the aperture walls. The higher the area ratio, the higher the transfer efficiency of the solder paste. Transfer efficiency is the percentage of solder paste printed into the aperture that is transferred onto the PCB pad. For paste with type-3 powder size, area ratio experiments have verified that apertures with area ratios of 0.66 or higher are able to print solder paste with transfer efficiencies above 60% with minimal print deposit volume variability (standard deviation ≤ 10%).

It is important to emphasize that transfer efficiencies and print volume variability for any stencil printing process is very much dependent upon the printing characteristics of the solder paste used. Based on work done with a lead-free no-clean solder paste with type-3 powder, the following general stencil design recommendations can be made:

- A 4 mil laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended.
- It is recommended that universal apertures be the same size as the pads on the PCB (1:1 aperture size to pad size ratio).
- If the universal apertures need to be reduced, reductions of up to 10% were found to be acceptable.
- It is recommended that space constrained apertures be the same size as the pads on the PCB (1:1 aperture size to pad size ratio).
- Reductions in the space constrained apertures should be avoided, but in those cases where a reduction is required, it should be kept to a minimum and not exceed 10%.

Solder Paste

For lead-free SMT assemblies, a lead-free no-clean solder paste with type-3 powder capable of printing fine features (paste should have good aperture release characteristics) is recommended.

Assembly Process

Package placement and alignment is dependent on placement equipment and process. Inaccurate placement may result in poor quality solder joints, solder shorts, or in devices being tilted and/or misaligned. Reflow experiments conducted with the MicroPak2™ package have shown that parts only slightly misaligned undergo automatic self-alignment during the reflow process. Self-centering behavior is very solder and process dependent and the customer should conduct experiments to confirm the limits of self centering with their specific solder paste and process.

Reflow Window

A system board reflow profile depends on the thermal mass of the entire assembly, so it is not practical to define a specific reflow profile just for the MicroPak2™ package. The recommendations made below with respect to reflow window and reflow profiles (Figure 2and Table 2) are meant to be guidelines to be customized for varying manufacturing practices and applications.

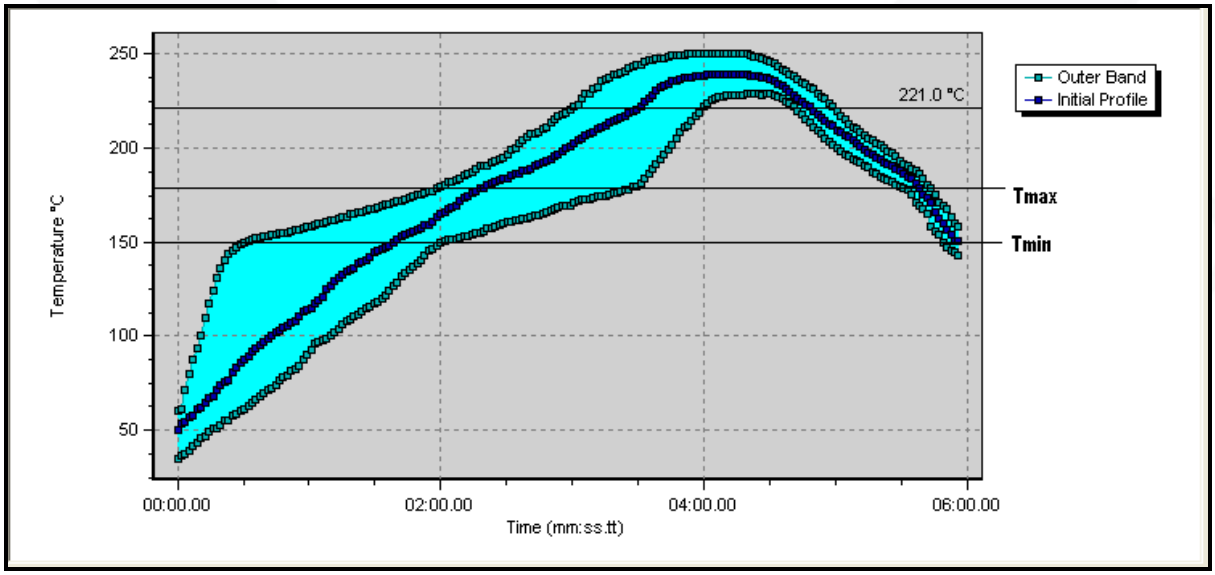

Figure 2. Acceptable Reflow Window

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Table 2. Reflow Window Parameters

Reflow Window Parameters	Pb-Free
Preheat:	
Temperature Min. (T_{MIN})	150°C
Temperature Max. (T_{MAX})	180°C
Time	45 to 90 seconds
Time above Liquidus (TAL):	
Temperature	221°C
Time	45 to 90 seconds
Time to Liquidus (TTL)	4 minutes maximum
Peak Temperature	235 – 250°C
Ramp-Up Rate	3°C/s maximum
Cool-Down Rate	6°C/s maximum

Table 3. Recommended Reflow Profile Parameters

Recommended Reflow Profile Parameters	Pb-Free
Preheat:	
Temperature Min. (T_{MIN})	150°C
Temperature Max. (T_{MAX})	180°C
Time	60-70 seconds
Time above Liquidus (TAL):	
Temperature	221°C
Time	60-70 seconds
Time to Liquidus (TTL)	4 minutes maximum
Peak Temperature	235 – 250°C
Ramp-Up Rate	3°C/s maximum
Cool-Down Rate	6°C/s maximum

Rework Guidelines

Solder joints are not fully exposed in the case of this package style, thereby limiting any form of "retouching." For defects underneath the package, the whole package needs to be removed. Rework of this style of leadless devices is challenging due to their small size. However, with care and dexterity and following the guidelines below, it can be accomplished.

The rework of this style of packages is further complicated by the types of products in which these components are used. They tend to be mounted on smaller, thinner, more-densely populated PCBs; challenging the rework technician due to part handling and heating difficulties. The proximity of parts adjacent to this package may further complicate this process. Due to the product-dependent complexities, the following provides only a guidelines and a starting point for the development of a successful rework process.

Inspection Guidelines

After PCB assembly, the package should be inspected using transmission X-ray for the presence of voids, solder balling, or other defects under the package. Cross sectioning may also be required to determine the fillet shape and size and the joint standoff height. *Refer to IPC inspection criteria for leadless devices found in IPC-A610 Rev D Section 8.2.13.*

Although this is a small leadless package, removal and replacement via a hot air rework process is recommended. The following steps are a guideline in developing a successful rework process for the particular PWB.

Process-Overalls

The process is as follows:

1. Component Removal
2. Site Redress
3. Bumping of PCB
4. Component placement and reflow
5. Inspection

Bake

Prior to rework, bake the PCB assembly at 125ºC for at least 24 hours to remove any residual moisture. Take care on temperature-sensitive components, coatings, etc.

Component Removal

The removal profile of the device should mimic as closely as possible the initial assembly profile. That being said, the time above liquidus can be reduced, as long as the reflow is complete, to speed up the entire rework process.

It is recommended that the PWB be heated from the bottom side (as shown in Figure 3) using a convective heater, and the topside with a hot gas nozzle, applying heat at the component to be removed. A thermocouple on the underside of the PWB should read 150°C as a minimum prior to beginning the removal process.

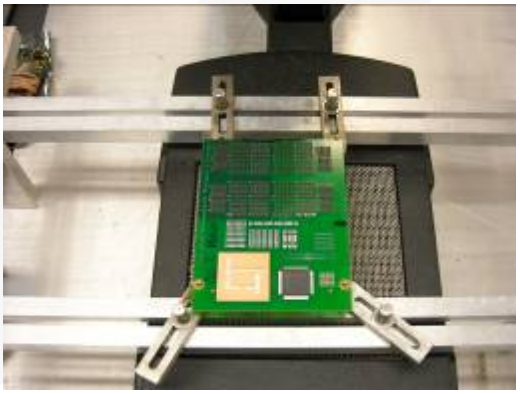

Figure 3. Bottom side heating of PCB

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Using a hot air source, remove the device by heating the area of the component. Then, using an ESD pair of tweezers, remove the device (as shown in Figure 4).

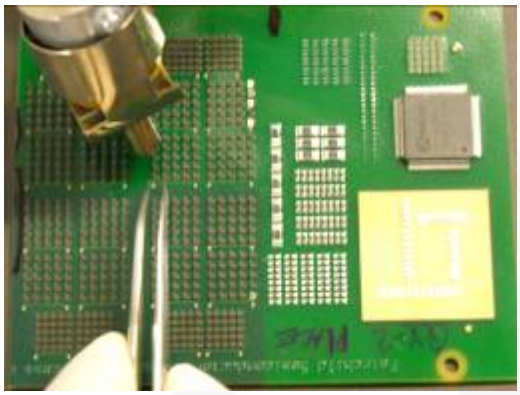

Figure 4. Removal of Device Using Hot Air Source

Heating of adjacent components should be minimized to avoid collateral damage both near and on the underside of the board (if components are populated in this area).

Once the joints have reflowed, remove the device with a vacuum pick- up (ESD safe) or tweezer. Due to the small package size, vacuum pressure should be kept below 15" of Hg to prevent premature board or pad lift before all joints have reflowed.

Site Cleaning

Clean the site on PWB properly, removing residual solder with a combination convection tip and de-soldering braid, as shown in Figure 5.

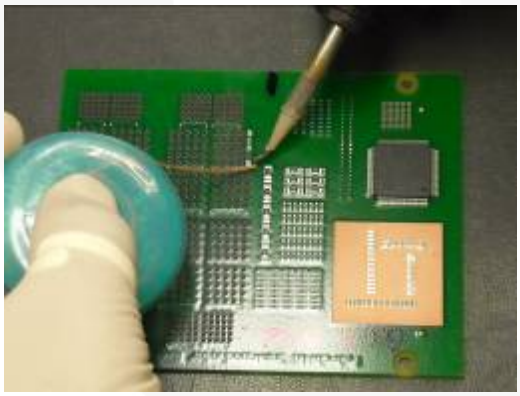

Figure 5. Solder Wicking, Site Prep

After residual solder removal, clean the lands with a cleaning agent specific to the original type of chemistries used in the original assembly.

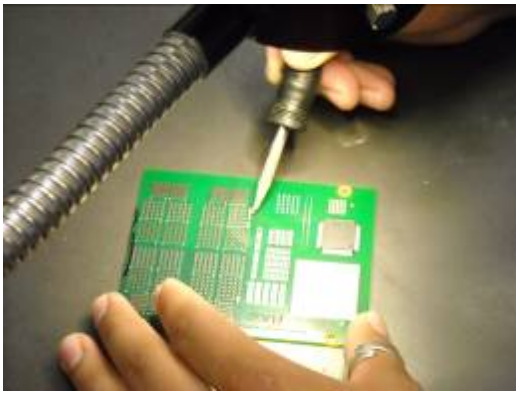

Figure 6. Solder "Bumping" of PCB Lands

Component Placement and Reflow-Method #1

"Bump" the pads of the PCB (shown in Figure 6 and Figure 7) by using the correct wire-cored solder and a hand-soldering iron using a small iron tip.

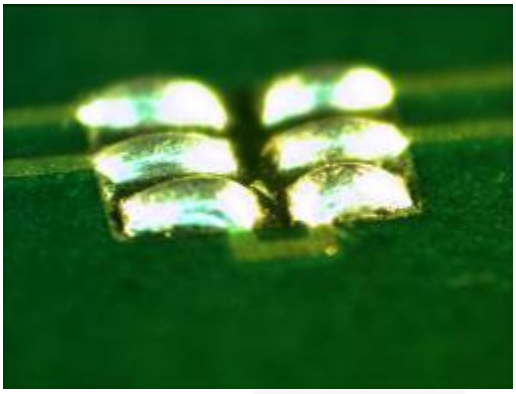

Figure 7. Figure 7-Solder "Bumped" Pads

Inspect to make the bumps on the board are uniform.

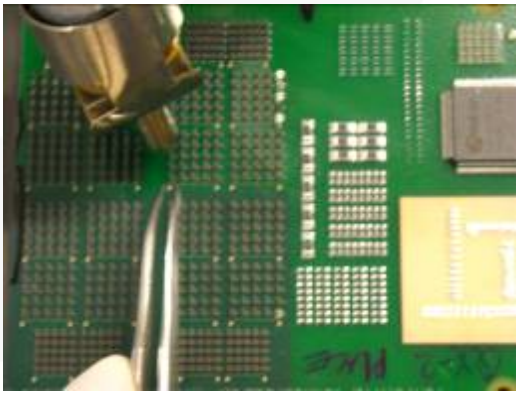

Figure 8. Heat Gun Reflow

Reflow the PCB using a hot air gun and a pair of tweezers to place the bumped device, as shown in Figure 8. This process requires using magnification.

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Alternatively, use a time-, distance-, and temperature-controlled hot-air source to do the rework using a time and controlled heat source. See Figure 9.

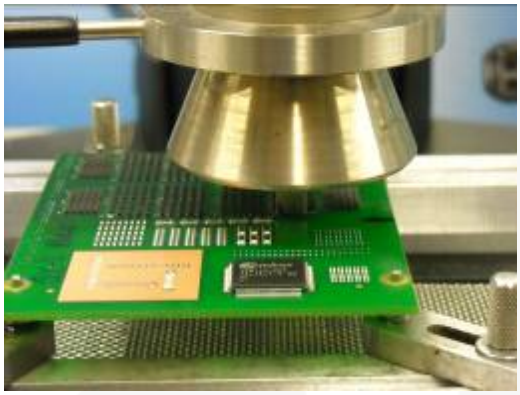

Figure 9. Hot Air Rework System Reflow

Reflow the PCB using the same profile as that developed for the initial attachment.

Cleaning

After placement and reflow, clean the lands with a cleaning agent specific to the original type of chemistries used in the original assembly.

Inspection

Inspect per the Inspection Guidelines discussed above.

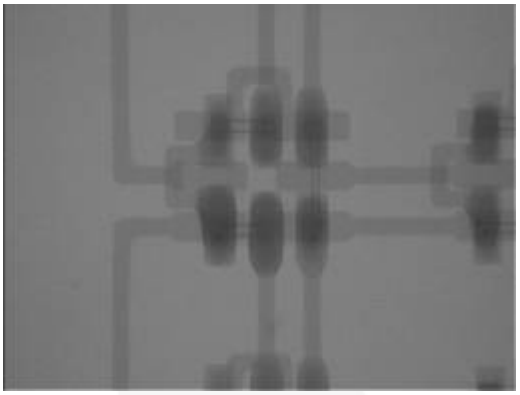

Figure 10.X-Ray Image of Leadless Device

References

Prepared by Cookson Electronics – Assembly Materials, 109 Corporate Blvd., South Plainfield, NJ 07080

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