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## GigaComm™ (SiGe) SPICE Modeling Kit



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### APPLICATION NOTE

#### Objective

The objective of this kit is to provide sufficient circuit schematic and SPICE parameter information to perform system level interconnect modeling for devices in ON Semiconductor’s high performance GigaComm (Silicon Germanium) logic family. The family has output edge rates as low as 20 ps and power supply levels of as low as 2.5 V. **The kit is not intended to provide information necessary to perform circuit level modeling on the GigaComm (SiGe) devices.**

#### Schematic Information

The kit contains representatives of input and output schematics, netlists, and waveform used for the GigaComm family devices. This application note will be modified as new devices are added. Table 1 describes the nomenclature used for modeling the schematic and netlist for GigaComm devices. The subcircuit models, such as input or output buffers, ESD and package simulate only device input or output paths. When used with interconnect models, a complete signal path may be modeled as shown in Figure 1.

Table 1. Schematics and Netlist Nomenclature

Parameter	Function Description
V <sub>CC</sub>	2.5/3.3 V for LVPECL and 0 V for LVECL
V <sub>EE</sub>	-2.5/-3.3 V for LVPECL and 0 V for LVECL
V <sub>BB</sub> or V <sub>MM</sub>	Output Voltage Reference (See Device Data Sheet)
V <sub>CS</sub>	Internally Generated Voltage ( $\approx V_{EE} + 1.1 \text{ V} \pm 50 \text{ mV}$ )*
GND	Ground 0 V
IN	True Input to CKT
INB	Inverted Input to CKT
Q	True Output of CKT
QB	Inverted Output of CKT

\*Note that the NBSG16VS, NBSG53A, NBSG72A, and NBSG86A are using V<sub>CS</sub> to modulate the output amplitude (see device specifics for more details).

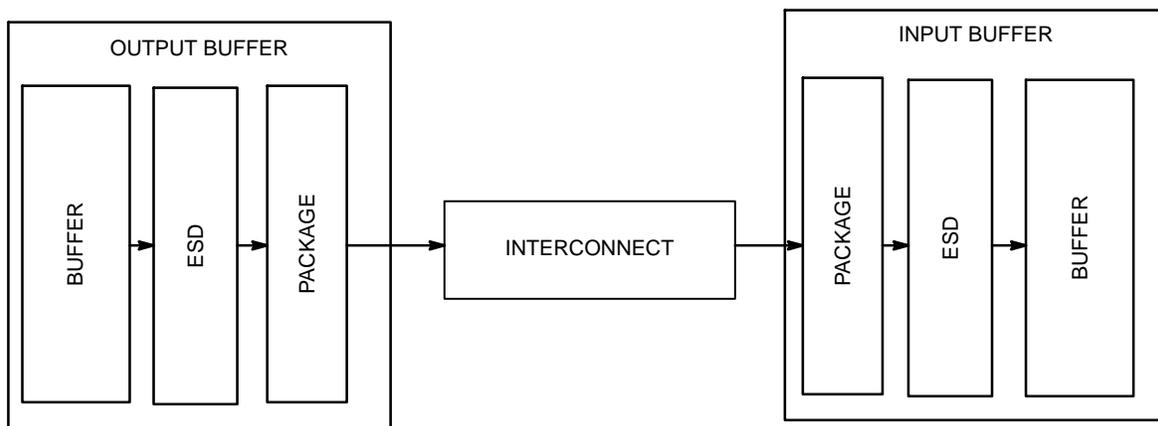


Figure 1. Interconnect Model Template

For device modeling, the behavioral LOGIC or gate functionality is not modeled (see Figure 2. DEVICE Model Template)

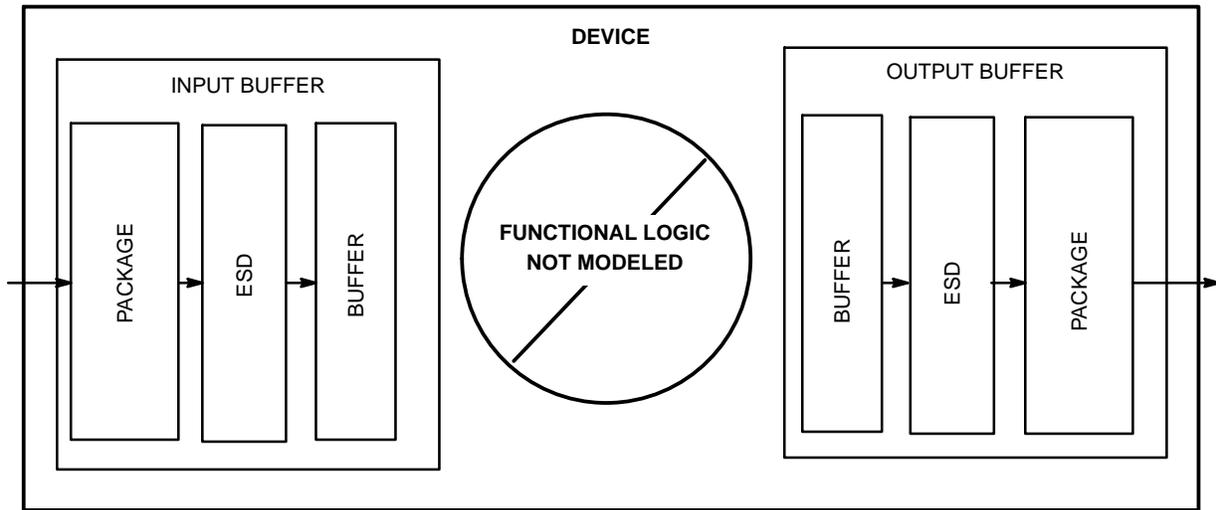


Figure 2. DEVICE Model Template

### Package

A worst-case model is included to improve the accuracy of the system model. The package model represents the parasitics as they are measured a sizable distance from an AC ground pin. The package models should be placed on all external inputs to an input model, all external outputs for an output model and the  $V_{CC}$  line. Since the current in the  $V_{EE}$  pin is a constant, a package model for  $V_{EE}$  pin is not necessary. Please note that an internal  $V_{CS}$  voltage does not require a package model.

To shorten and speed up the simulation process, the simplified package model should be used. The input and output buffers schematic include the simplified QFN package model (Figures 4, 5, and 8).

### Input Buffer

The “SG\_INBUF” schematic and netlist are representing the input structures of devices for GigaComm family devices. The schematics require the addition of ESD and package models to be accurate; but are otherwise functionally correct. It is unnecessary to include an ESD or Package model for the  $V_{BB}$  or  $V_{MM}$  type pins of the models because  $V_{BB}$  type input is intended as an internal node for most applications. If a  $V_{BB}$  type input is modeled as an external node it is usually bypassed because it is a constant voltage, and adding ESD and Package parameters provide no additional benefit.

### Output Buffer

Two output buffer schematics and netlists are modeled and can be seen on pages 6 and 8. The package models with all parasitics should be added for better accuracy. Any input or output that is driving or being driven by an off chip signal should include the ESD and package models. Open or floating pins will not require any ESD or package models. The output buffer models typically show internal differential inputs and outputs and should always be simulated with both output lines terminated, even when only one line or single ended use is intended. This will balance the output buffer’s load.

### Example of the Typical Interconnect Circuit

The output signal buffer SG\_0BUF\_01 with the ESD protection structure and the simplified package model properly terminated, driving the simplified input structure is shown in the Figure 13. The circuit provides working schematics of complete interconnect modeling. The output waveform observed at the receiver of the interconnect example is shown in the Figure 14.

### SPICE Netlist

The netlists are organized as a group of subcircuits. In each subcircuit model netlist, the model name should be followed by a list of external node interconnects. When copying “SUBCKT” netlist files to your text editor, use Adobe® Acrobat® Reader® 4.0 or higher to ensure proper conversion.

### SPICE Parameter Information

In addition to the schematics and netlists there is a listing of the SPICE parameters for the transistors referenced in the schematics and netlists. These parameters represent a typical device of a given transistor. Varying the typical parameters will affect the DC and AC performance of the structures; but for the type of modeling intended by this note, the actual delay times are not necessary and are not modeled, as a result variation of the device parameters are meaningless. The performance levels are more easily varied by other methods and will be discussed in the next section. The resistors referenced in the schematics are polysilicon and have no parasitic capacitance in the real circuit and none is required in the model. The schematics display only the devices needed in the SPICE netlists.

### Modeling Information

The bias drivers for the devices are not included as they are unnecessary for interconnect simulations and their use results in a large increase in model complexity and simulation time. The internal reference voltages ( $V_{BB}$ ,  $V_{CS}$ , etc.) should be driven with ideal constant voltage sources. If a GigaComm device is used in positive mode the levels vary one to one with the power supply; but are constant as a function of temperature.

The schematics and SPICE parameters will provide a typical output waveform, which can be seen in Figures 9 and 10. Note that ESD and package models will add 5 ps–7 ps to rise and fall time of the output waveform. Simple adjustments can be made to the models allowing output characteristics to simulate conditions at or near the corners of the data book specifications. Consistent cross-point voltages need to be maintained.

- **To adjust rise and fall times:**

Produce the desired rise and fall times output slew rates by adjusting collector load resistors to change the gates tail current. The  $V_{CS}$  voltage will affect the tail current in the output differential, which will interact with the load resistor and collector resistor to determine  $t_r$  and  $t_f$  at the output.

- **To adjust the  $V_{OH}$ :**

Adjust the  $V_{OH}$  and  $V_{OL}$  level by the same amount by varying  $V_{CC}$ . The output levels will follow changes in  $V_{CC}$  at a 1:1 ratio.

- **To adjust the  $V_{OL}$  only:**

Adjust the  $V_{OL}$  level independently of the  $V_{OH}$  level by increasing or decreasing the collector load resistance. Note that the  $V_{OH}$  level will also change slightly due to an  $I_{BASE} R$  drop across the collector load resistor. The  $V_{OL}$  can be changed by varying the  $V_{CS}$  supply, and therefore the gate current through the current source resistor.

### Device Specifics

#### NBSG16VS

The NBSG16VS is a differential receiver/driver with variable output amplitude which is controlled by a voltage applied to  $V_{CTRL}$  over the range of  $V_{CC}$  to  $V_{CC} - 2$  V. These  $V_{CTRL}$  voltages produce corresponding output amplitudes over the range of 75 mV to 750 mV (see Data Sheet Figure 11). The SPICE model for NBSG16VS simulates seven selected swings within the output amplitude range by adjusting  $V_{CS}$  to one of seven voltages per Table 2. Simulation tr/tf represents the worst case (fastest) edges. A DC offset must be applied to all voltages to convert LVNECL to LVPECL at a 1:1 ratio.

#### NBSG53A, NBSG72A, and NBSG86A

The NBSG53A, NBSG72A, and NBSG86A are multifunctional differential GigaComm devices with Output Level Select (OLS) capability. The OLS input pin is used to program the peak-to-peak output amplitude between 0 mV and 800 mV in five discrete steps. When simulating output of the NBSG53A, NBSG72A, or NBSG86A, use Table 2,  $V_{CS}$  value from line 3, 5, 7, or 10 to obtain desired output amplitude swing.

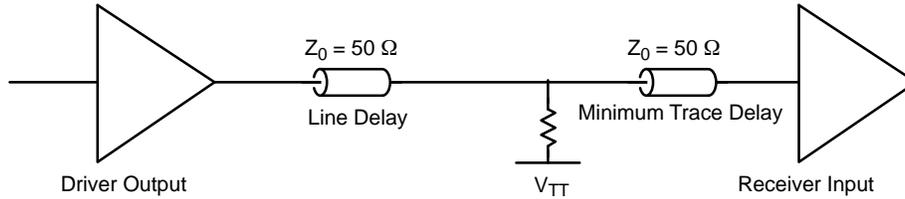
**Table 2. Required  $V_{CS}$  for Selected Output Amplitudes of the NBSG16VS**

	Output Amplitude (mV)	$V_{CS}$ (V)
1.	75	$V_{EE} + 0.865$
2.	100	$V_{EE} + 0.9$
3.	200	$V_{EE} + 0.98$
4.	300	$V_{EE} + 1.06$
5.	400	$V_{EE} + 1.15$
6.	500	$V_{EE} + 1.23$
7.	600	$V_{EE} + 1.3$
8.	700	$V_{EE} + 1.38$
9.	750	$V_{EE} + 1.42$
10.	800	$V_{EE} + 1.46$

**Summary**

The information included in this kit provides adequate information to run a SPICE level system interconnect simulation. The block diagram in Figure 3 illustrates a

typical situation, which can be modeled using the information in this kit. Device input or output models are presented in Table 3.



**Figure 3. Typical Application for I/O SPICE Modeling Kit**

**Table 3. GigaComm Input/Output Buffer Selector Guide**

Device	Function	Input Model	Output Model
NB7L11M	2.5/3.3 V 1:2 Differential Clock/Data Driver with CML Outputs	SG_INBUF	SG_OBUF_02
NB7L14M	2.5/3.3 V 1:4 Differential Clock/Data Driver with CML Outputs	SG_INBUF	SG_OBUF_02
NB7L86M	2.5/3.3 V Differential Smart Gate with CML Outputs	SG_INBUF	SG_OBUF_02
NBSG11	2.5/3.3 V Differential Clock Driver with RSECL Outputs	SG_INBUF	SG_OBUF_01
NBSG14	2.5/3.3 V Differential Receiver/Driver with RSECL Outputs	SG_INBUF	SG_OBUF_01
NBSG16	2.5/3.3 V Differential Receiver/Driver with RSECL Outputs	SG_INBUF	SG_OBUF_01
NBSG16VS	2.5/3.3 V Differential Receiver/Driver with Variable Output Swing	SG_INBUF	SG_OBUF_01*
NBSG16M	2.5/3.3 V Differential CML Receiver/Driver	SG_INBUF	SG_OBUF_02
NBSG53A	2.5/3.3 V Selectable Differential Clock and Data D Flip-Flop/Clock Divider with Reset and OLS	SG_INBUF	SG_OBUF_01*
NBSG72A	3.5/3.3 V Differential CML 2x2 Crosspoint Switch with OLS	SG_INBUF	SG_OBUF_01*
NBSG86A	2.5/3.3 V Differential Smart Gate with OLS	SG_INBUF	SG_OBUF_01*

\*Note: See Device Specifics and Table 2 for Details.

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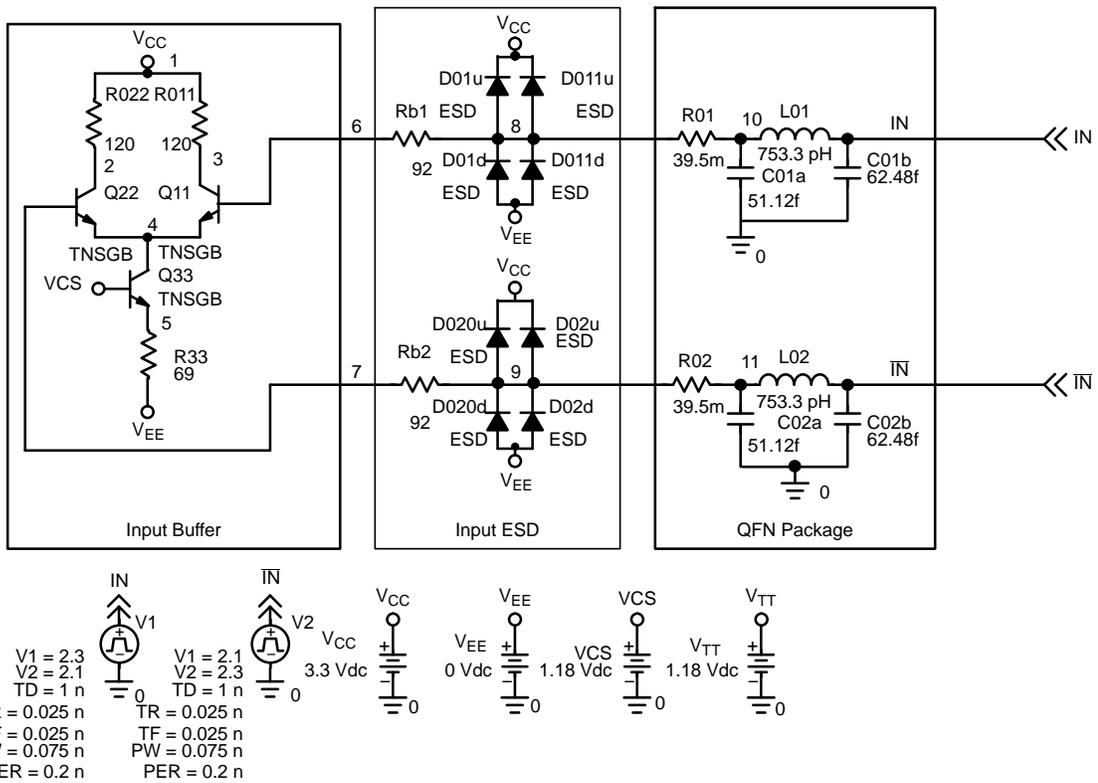


Figure 4. Simplified Input Circuitry – SG\_INBUF

```

.SUBCKT SG_INBUF IN INB VCC VEE VCS
Q_Q11      3 6 4 TNSGB
Q_Q22      2 7 4 TNSGB
Q_Q33      4 VCS 5 TNSGB
R_R011     3 VCC 120
R_R022     2 VCC 120
R_R33      VEE 5 69
R_Rb1      6 8 92
R_Rb2      9 7 92
R_R01      8 10 39.5m
R_R02      9 11 39.5m
L_L01      10 IN 753.3pH
L_L02      11 INB 753.3pH
D_D01d     VEE 8 ESD
D_D011d    VEE 8 ESD
D_D02d     VEE 9 ESD
D_D020d    VEE 9 ESD
D_D01u     8 VCC ESD
D_D011u    8 VCC ESD
D_D02u     9 VCC ESD
D_D020u    9 VCC ESD
C_C01a     0 10 51.12f
C_C02a     0 11 51.12f
C_C01b     0 IN 62.48f
C_C02b     0 INB 62.48f
V_VCC      VCC 0 3.3Vdc
V_VCS      VCS 0 1.18Vdc
V_VEE      VEE 0 0Vdc
V_V1       IN 0 PULSE 2.3 2.1 1n 0.025n 0.025n 0.075n 0.2n
V_V2       INB 0 PULSE 2.1 2.3 1n 0.025n 0.025n 0.075n 0.2n
.END SG_INBUF
  
```

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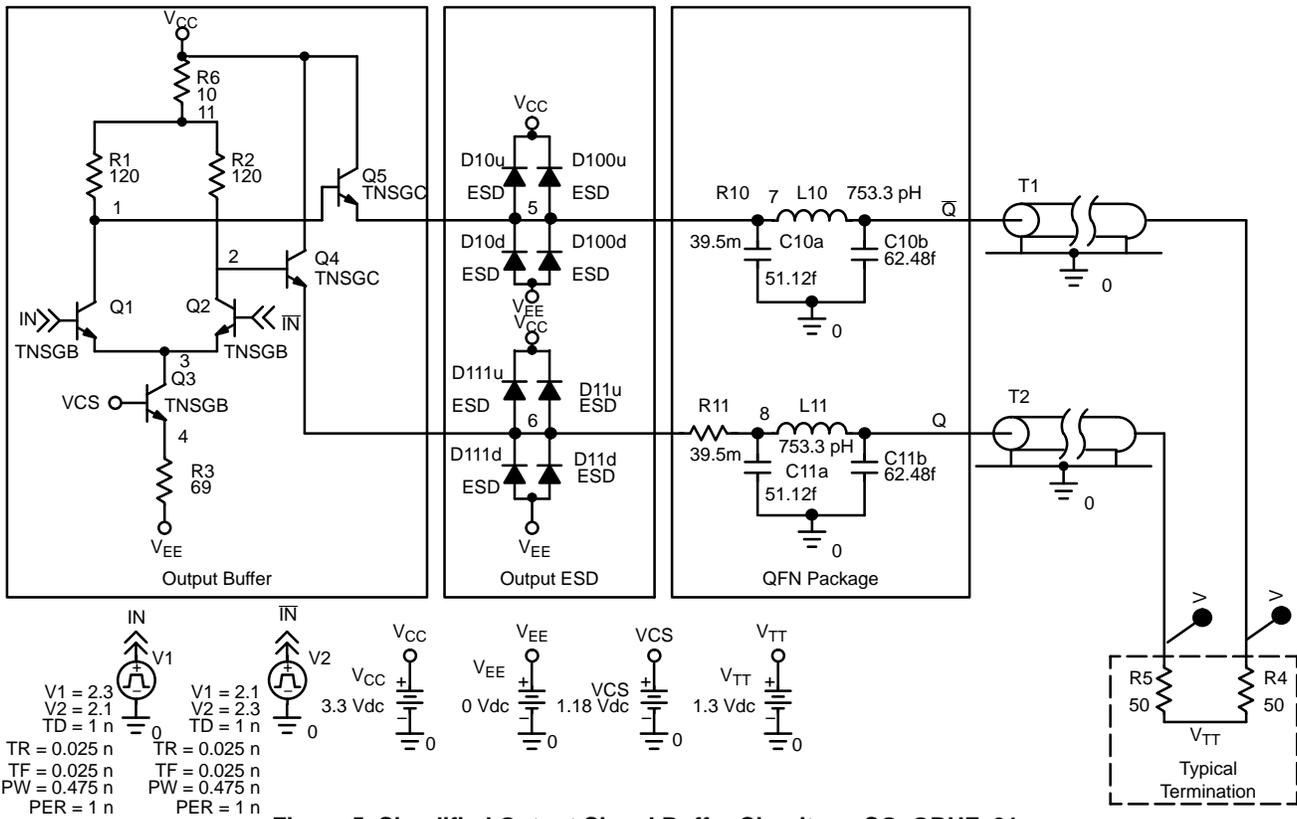
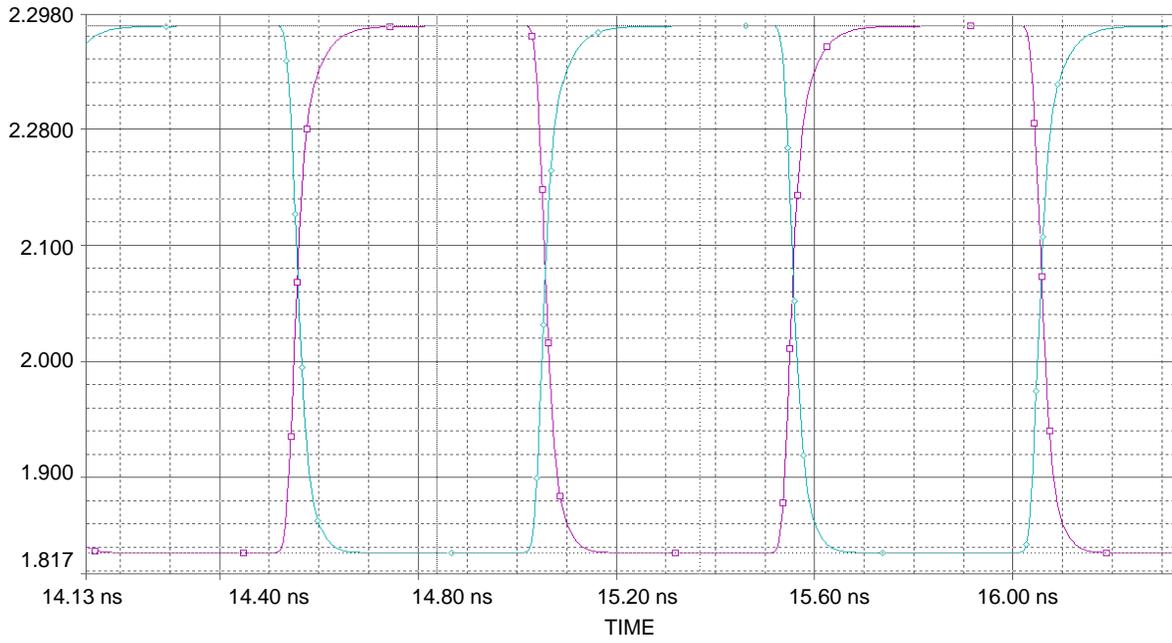


Figure 5. Simplified Output Signal Buffer Circuitry – SG\_OBUF\_01

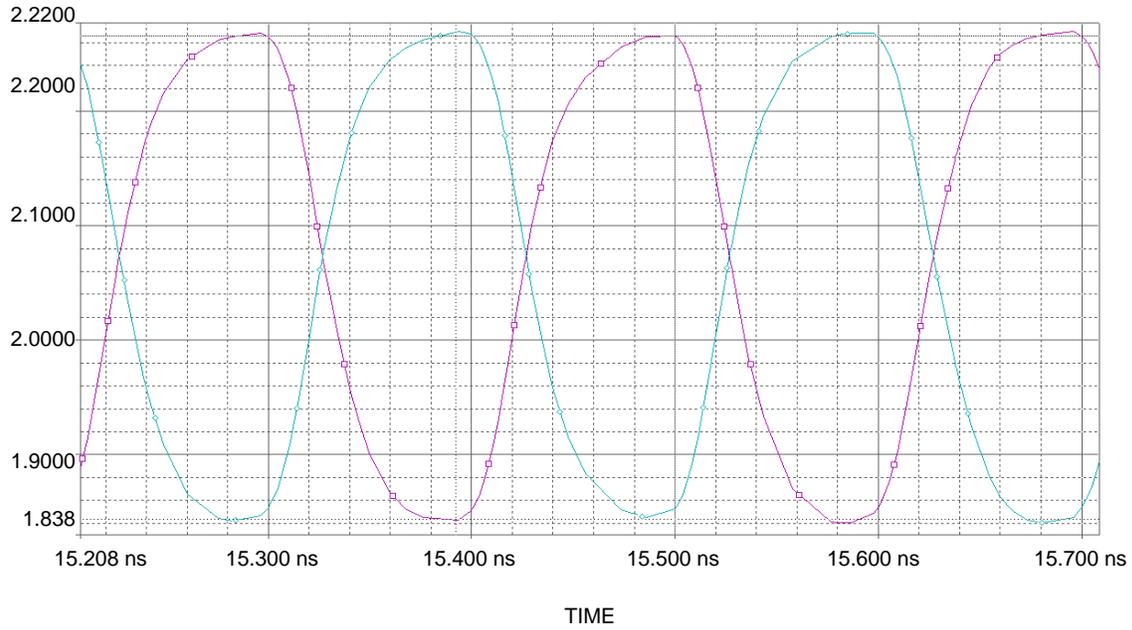
```

.SUBCKT SG_OBUF_01 IN INB VCC VEE VTT VCS Q QB
Q_Q1      1 IN 3 TNSGB
Q_Q2      2 INB 3 TNSGB
Q_Q3      3 VCS 4 TNSGB
Q_Q4      VCC 2 6 TNSGC
Q_Q5      VCC 1 5 TNSGC
R_R1      1 11 120
R_R2      2 11 120
R_R3      VEE 4 69
R_R4      10 VTT 50
R_R5      9 VTT 50
R_R6      11 VCC 10
R_R10     5 7 39.5m
R_R11     6 8 39.5m
C_C10b    0 QB 62.48f
C_C11a    0 8 51.12f
C_C11b    0 Q 62.48f
C_C10a    0 7 51.12f
L_L10     7 QB 753.3pH
L_L11     8 Q 753.3pH
D_D111d   VEE 6 ESD
D_D111u   6 VCC ESD
D_D100u   5 VCC ESD
D_D10u    5 VCC ESD
D_D11u    6 VCC ESD
D_D100d   VEE 5 ESD
D_D10d    VEE 5 ESD
D_D11d    VEE 6 ESD
V_VCC     VCC 0 3.3Vdc
V_VCS     VCS 0 1.18Vdc
V_VTT     VTT 0 1.3Vdc
V_VEE     VEE 0 0Vdc
V_V1      IN 0 PULSE 2.3 2.1 1n 0.025n 0.025n 0.075n 0.2n
V_V2      INB 0 PULSE 2.1 2.3 1n 0.025n 0.025n 0.075n 0.2n
T_T1     QB 0 10 0 Z0=50 TD=80ps
T_T2     Q 0 9 0 Z0=50 TD=80ps
.END SG_OBUF_01
  
```

# AND8077/D



**Figure 6. Typical Output Waveform of the SG\_OBUF\_01 at 1 GHz**  
( $t_r = 34$  ps,  $t_f = 32$  ps,  $V_{outpp} = 451$  mV,  $V_{oh} = 2.288$  V,  $V_{ol} = 1.835$  V)



**Figure 7. Typical Output Waveform of the SG\_OBUF\_01 at 5 GHz**  
( $t_r = 32$  ps,  $t_f = 30$  ps,  $V_{outpp} = 422$  mV,  $V_{oh} = 2.26$  V,  $V_{ol} = 1.84$  V)

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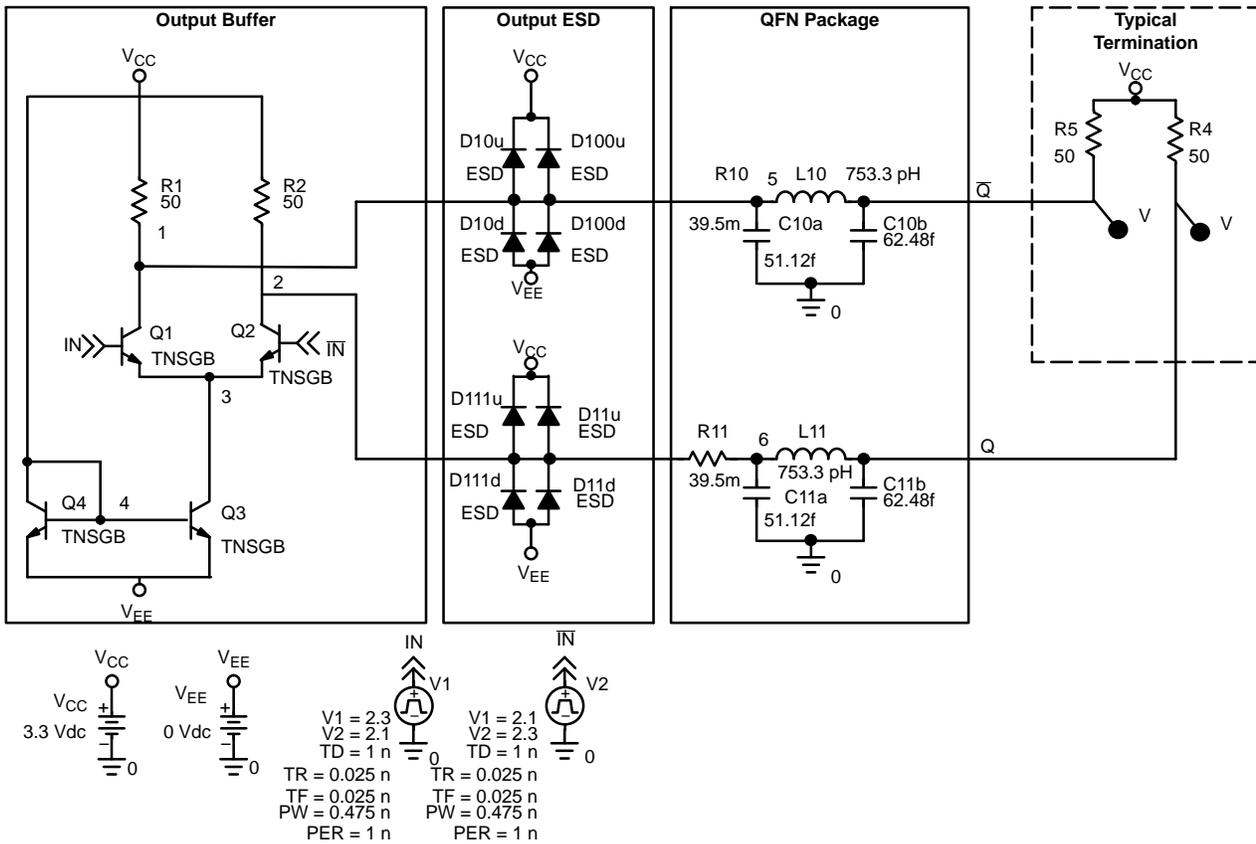
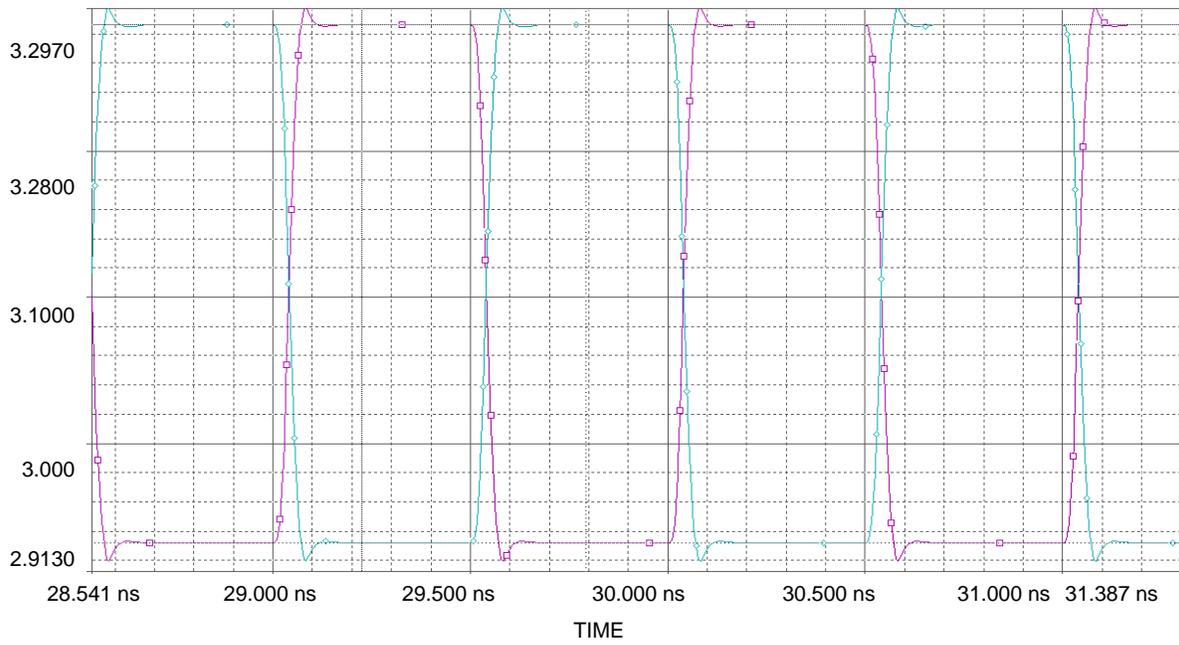


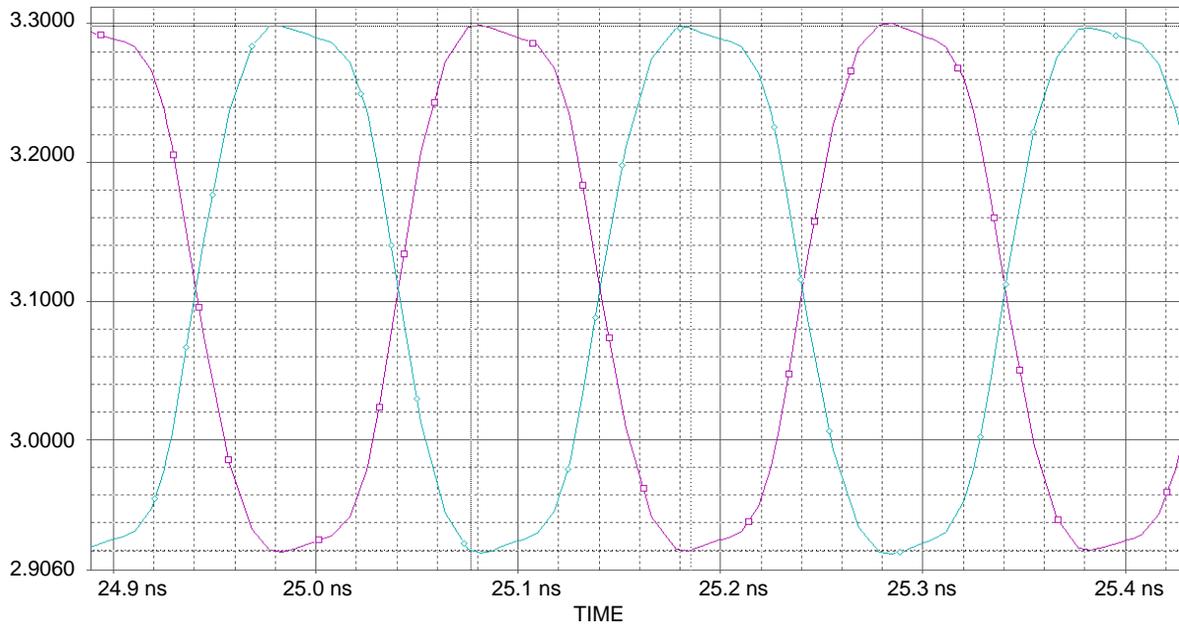
Figure 8. Simplified Output Signal Buffer Circuitry – SG\_OBUF\_02

```
.SBUCKT SG_OBUF02 IN INB VEE VCC VCS Q QB
Q_Q1      1 IN 3 TNSGB
Q_Q2      2 INB 3 TNSGB
Q_Q3      3 4 VEE TNSGB
Q_Q4      4 4 VEE TNSGB
R_R1      1 VCC 50
R_R2      2 VCC 50
R_R3      QB VCC 50
R_R4      Q VCC 50
R_R10     1 5 39.5m
R_R11     2 6 39.5m
L_L10     5 QB 753.3pH
L_L11     6 Q 753.3pH
C_C10b    0 QB 62.48f
C_C10a    0 5 51.12f
C_C11a    0 6 51.12f
C_C11b    0 Q 62.48f
D_D10d    VEE 1 ESD
D_D11d    VEE 2 ESD
D_D111u   2 VCC ESD
D_D111d   VEE 2 ESD
D_D100u   1 VCC ESD
D_D10u    1 VCC ESD
D_D11u    2 VCC ESD
D_D100d   VEE 1 ESD
V_VEE     VEE 0 0Vdc
V_VCC     VCC 0 3.3Vdc
I_I1      VCC 4 DC 16mAdc
V_V1      IN 0 PULSE 2.3 2.1 1n 0.025n 0.025n 0.475n 1n
V_V2      INB 0 PULSE 2.1 2.3 1n 0.025n 0.025n 0.475n 1n
.END SG_OBUF02
```

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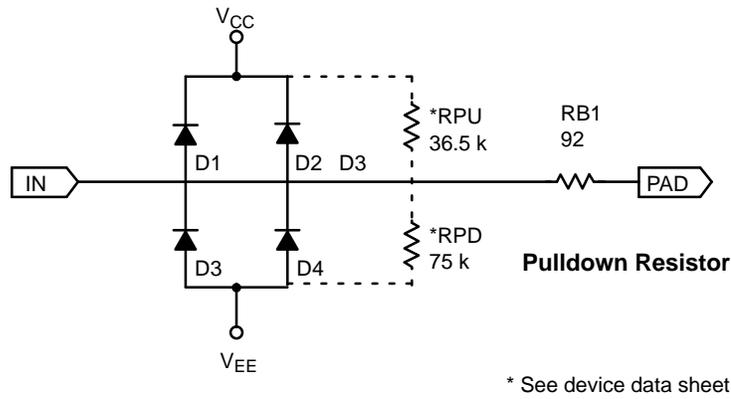


**Figure 9. Typical Output Waveform of the SG\_OBUF\_02 at 1 GHz  
( $t_r = 30$  ps,  $t_f = 28$  ps,  $V_{outpp} = 354$  mV,  $V_{oh} = 3.29$  V,  $V_{ol} = 2.93$  V)**



**Figure 10. Typical Output Waveform of the SG\_OBUF\_02 at 5 GHz  
( $t_r = 29$  ps,  $t_f = 28$  ps,  $V_{outpp} = 364$  mV,  $V_{oh} = 3.29$  V,  $V_{ol} = 2.92$  V)**

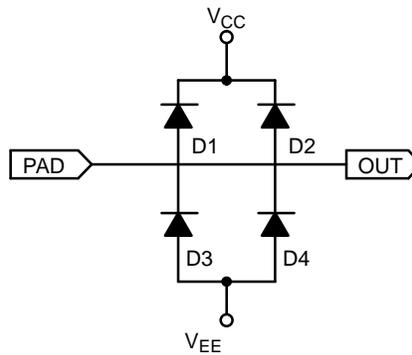
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\* See device data sheet

**Figure 11. Input ESD**

```
.SUBCKT IN_ESD VCC VEE IN PAD
D1 IN VCC ESD
D2 IN VCC ESD
D3 VEE IN ESD
D4 VEE IN ESD
-----
RPD IN VEE 75K
RPU IN VCC 36.5K
RB1 IN PAD 92
.ENDS IN_ESD
```



**Figure 12. Output ESD**

```
.SUBCKT OUT_ESD VCC VEE OUT
D1 OUT VCC ESD
D2 OUT VCC ESD
D3 VEE OUT ESD
D4 VEE OUT ESD
.ENDS OUT_ESD
```

\*\*\*\*\*Transistor and Diode Models for GigaComm\*\*\*\*\*

```
.MODEL TNSGC NPN (IS=1.47e-16 BF=180 NF=1 VAF=96.3 IKF=1.62e-01
ISE=2.96e-15 NE=2.5 BR=20.2 VAR=2.76 IKR=1.34e-02 ISC=2.14e-16
NC=1.426 RB=25 IRB=1.50e-03 RBM=4 RE=1 RC=7 CJE=3.34e-15
VJE=.8867 MJE=.2868 TF=2.00e-12 ITF=0.25e-01 XTF=0.7 VTF=0.35 PTF=20 TR=0.5e-9 CJC=1.08e-15
VJC=0.632 MJC=0.301 XCJC=.3 CJS=8.12e-16 VJS=.4193 MJS=0.256 EG=1.119 XTI=3.999 XTB=0.8826
FC=0.9)
```

```
.MODEL TNSGB NPN (IS=2.18e-17 BF=179 NF=1 VAF=96.5 IKF=2.42e-02
ISE=3.83e-16 NE=2.5 BR=20.4 VAR=2.76 IKR=1.98e-03 ISC=2.91e-17
NC=1.426 RB=55 IRB=1.12e-04 RBM=48 RE=6 RC=11 CJE=4.98e-16
VJE=.8867 MJE=.2868 TF=2.00e-12 ITF=0.4e-02 XTF=0.7 VTF=0.6 PTF=20
TR=0.5e-9 CJC=1.55e-16 VJC=0.632 MJC=0.301 XCJC=0.3 CJS=1.71e-16 VJS=.4193 MJS=0.256
EG=1.119 XTI=3.999 XTB=0.8826 FC=0.9)
```

```
.MODEL ESD D (IS=9.99E-21 CJO=65.2E-15 RS=50.1 VJ=0.82 M=0.25 BV= 35)
```

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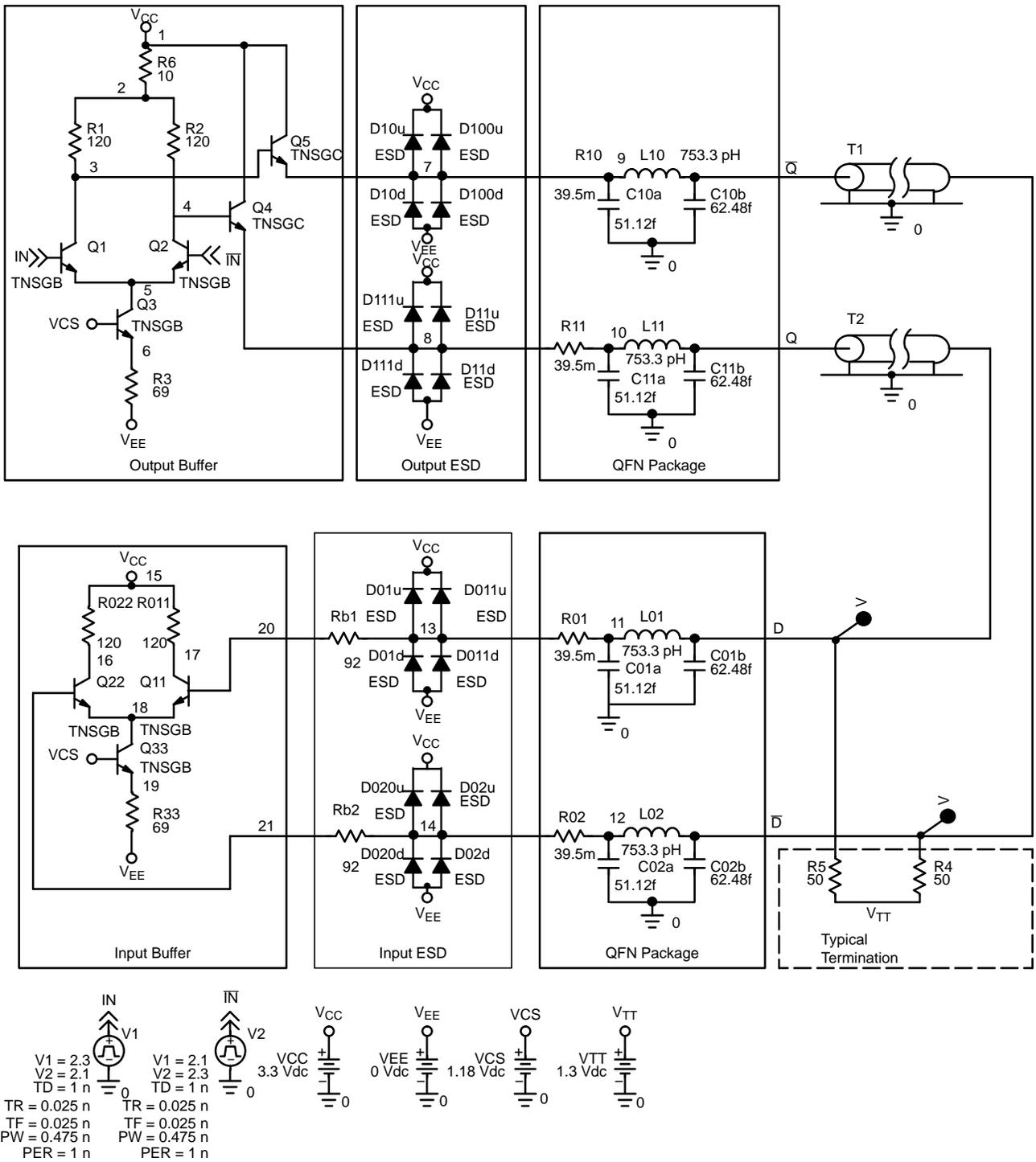
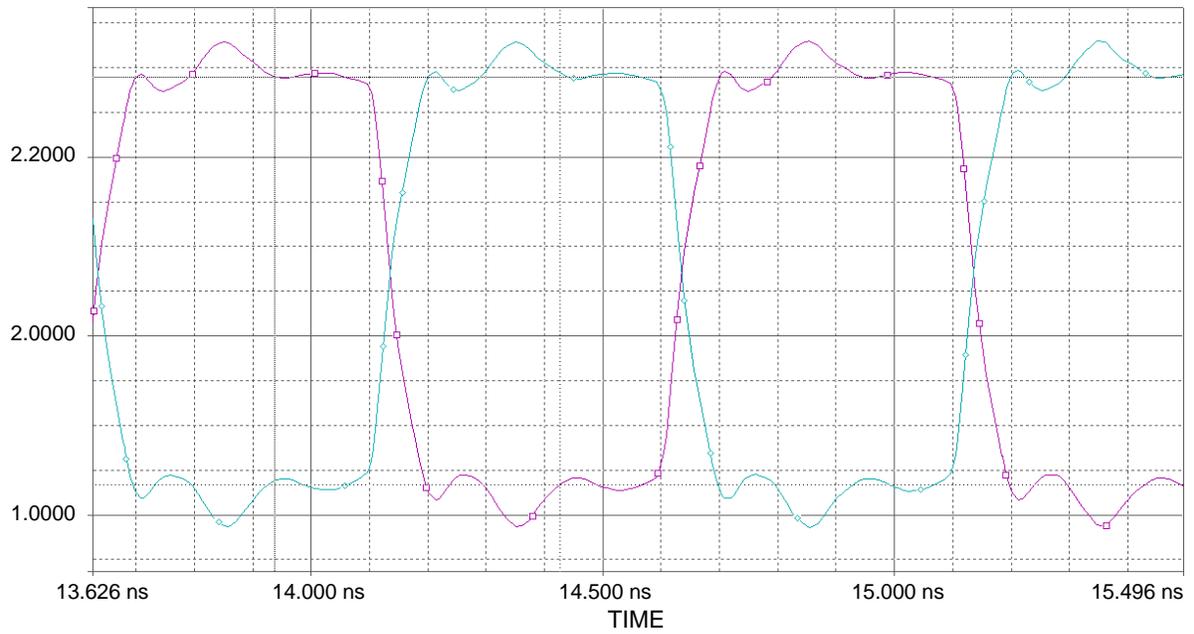


Figure 13. Example of the Typical Interconnect Circuit

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**Figure 14. Output Waveform of the Interconnect Example Shown in Figure 13  
(Frequency = 1 GHz,  $t_r = 49$  ps,  $t_f = 53$  ps,  $V_{outpp} = 455$  mV)**

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```

-----
* Package: 16 pin QFN
* Model for 16 pins
*
* Note:
* 1. The model assumes ground plane is 15 mil below package
* 2. The model assumes flag is grounded
* 3. The model is based on GigaComm device 1.475mm x 1.475mm
* 4. Wire bond parasitics are lumped with lead frame post.
* 5. Lump element equivalent model valid up to 10 Ghz
*****
* Lead Frame drawing: ASAT 3mm x 3mm QFN
* Case Outline:
* LC file : 16qfn3x3.LC
*****
*
* Package: GigaComm 16 pin 3mm x 3mm QFN
* Model for 16 pins
*
*
* Conductor number-pin designation cross reference:
*
*   Conductor      Pin
*   -----
*   1              1
*   2              2
*   3              3
*   4              4
*   5              5
*   6              6
*   7              7
*   8              8
*   9              9
*   10             10
*   11             11
*   12             12
*   13             13
*   14             14
*   15             15
*   16             16
*
* number of lumps: 1
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
.SUBCKT PACKAGE N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O N09I N09O
+ N10I N10O N11I N11O N12I N12O N13I N13O N14I N14O
+ N15I N15O N16I N16O BD_GND
R01  N01I  N01C  4.300e-02
C01a  N01C  BD_GND  6.674e-14
C01b  N01O  BD_GND  8.157e-14
L01  N01C  N01O  8.418e-10
R02  N02I  N02  3.950e-02
C02a  N02C  BD_GND  5.153e-14
C02b  N02O  BD_GND  6.298e-14
L02  N02C  N02O  7.557e-10
R03  N03I  N03C  3.950e-02
C03a  N03C  BD_GND  5.364e-14
C03b  N03O  BD_GND  6.556e-14
L03  N03C  N03O  7.550e-10
R04  N04I  N04C  4.300e-02
C04a  N04C  BD_GND  6.687e-14
C04b  N04O  BD_GND  8.173e-14

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L04	N04C	N04O	8.427e-10
R05	N05I	N05C	4.300e-02
C05a	N05C	BD_GND	6.633e-14
C05b	N05O	BD_GND	8.107e-14
L05	N05C	N05O	8.451e-10
R06	N06I	N06C	3.950e-02
C06a	N06C	BD_GND	5.202e-14
C06b	N06O	BD_GND	6.358e-14
L06	N06C	N06O	7.560e-10
R07	N07I	N07C	3.950e-02
C07a	N07C	BD_GND	5.243e-14
C07b	N07O	BD_GND	6.408e-14
L07	N07C	N07O	7.551e-10
R08	N08I	N08C	4.300e-02
C08a	N08C	BD_GND	6.682e-14
C08b	N08O	BD_GND	8.168e-14
L08	N08C	N08O	8.432e-10
R09	N09I	N09C	4.300e-02
C09a	N09C	BD_GND	6.606e-14
C09b	N09O	BD_GND	8.074e-14
L09	N09C	N09O	8.418e-10
R10	N10I	N10C	3.950e-02
C10a	N10C	BD_GND	5.112e-14
C10b	N10O	BD_GND	6.248e-14
L10	N10C	N10O	7.533e-10
R11	N11I	N11C	3.950e-02
C11a	N11C	BD_GND	5.166e-14
C11b	N11O	BD_GND	6.314e-14
L11	N11C	N11O	7.524e-10
R12	N12I	N12C	4.300e-02
C12a	N12C	BD_GND	6.786e-14
C12b	N12O	BD_GND	8.294e-14
L12	N12C	N12O	8.415e-10
R13	N13I	N13C	4.300e-02
C13a	N13C	BD_GND	6.628e-14
C13b	N13O	BD_GND	8.101e-14
L13	N13C	N13O	8.426e-10
R14	777N14I	N14C	3.950e-02
C14a	N14C	BD_GND	5.238e-14
C14b	N14O	BD_GND	6.402e-14
L14	N14C	N14O	7.536e-10
R15	N15I	N15C	3.950e-02
C15a	N15C	BD_GND	5.310e-14
C15b	N15O	BD_GND	6.490e-14
L15	N15C	N15O	7.514e-10
R16	N16I	N16C	4.300e-02
C16a	N16C	BD_GND	6.692e-14
C16b	N16O	BD_GND	8.179e-14
L16	N16C	N16O	8.412e-10
K0102	L01	L02	0.1711
C0102a	N01C	N02C	1.740e-14
C0102b	N01O	N02O	2.126e-14
K0103	L01	L03	0.0676
K0115	L01	L15	0.0549
K0116	L01	L16	0.1085
C0116a	N01C	N16C	4.797e-15
C0116b	N01O	N16O	5.863e-15
K0203	L02	L03	0.1574
C0203a	N02C	N03C	1.622e-14
C0203b	N02O	N03O	1.983e-14
K0204	L02	L04	0.0690
K0216	L02	L16	0.0555

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K0304	L03	L04	0.1713
C0304a	N03C	N04C	1.744e-14
C0304b	N03O	N04O	2.131e-14
K0305	L03	L05	0.0563
K0405	L04	L05	0.1098
C0405a	N04C	N05C	4.747e-15
C0405b	N04O	N05O	5.803e-15
K0406	L04	L06	0.0560
K0506	L05	L06	0.1723
C0506a	N05C	N06C	1.739e-14
C0506b	N05O	N06O	2.125e-14
K0507	L05	L07	0.0695
K0607	L06	L07	0.1578
C0607a	N06C	N07C	1.633e-14
C0607b	N06O	N07O	1.996e-14
K0608	L06	L08	0.0676
K0708	L07	L08	0.1708
C0708a	N07C	N08C	1.748e-14
C0708b	N07O	N08O	2.136e-14
K0709	L07	L09	0.0551
K0809	L08	L09	0.1085
C0809a	N08C	N09C	4.797e-15
C0809b	N08O	N09O	5.863e-15
K0810	L08	L10	0.0555
K0910	L09	L10	0.1711
C0910a	N09C	N10C	1.734e-14
C0910b	N09O	N10O	2.119e-14
K0911	L09	L11	0.0684
K1011	L10	L11	0.1574
C1011a	N10C	N11C	1.613e-14
C1011b	N10O	N11O	1.972e-14
K1012	L10	L12	0.0673
K1112	L11	L12	0.1711
C1112a	N11C	N12C	1.751e-14
C1112b	N11O	N12O	2.139e-14
K1113	L11	L13	0.0558
K1213	L12	L13	0.1097
C1213a	N12C	N13C	4.797e-15
C1213b	N12O	N13O	5.863e-15
K1214	L12	L14	0.0561
K1314	L13	L14	0.1715
C1314a	N13C	N14C	1.748e-14
C1314b	N13O	N14O	2.136e-14
K1315	L13	L15	0.0678
K1415	L14	L15	0.1573
C1415a	N14C	N15C	1.636e-14
C1415b	N14O	N15O	2.000e-14
K1416	L14	L16	0.0682
K1516	L15	L16	0.1707
C1516a	N15C	N16C	1.748e-14
C1516b	N15O	N16O	2.137e-14

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